

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 AND

BS CECC 90103 - 102

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ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:

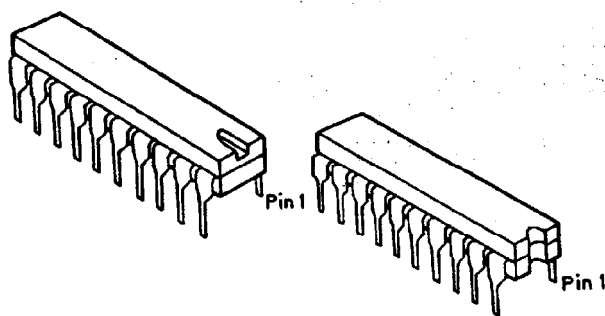
BS CECC 90 000 : 1976
BS CECC 90 100 : 1977

MANUFACTURERS TYPE NUMBER

54LS273
64LS273
74LS273
84LS273

Outline not to scale: Isometric projection
Marking information see clause 1

SEE PD 9002 AND CECC 00 200
For ordering information see
clause 1



OCTAL D-TYPE BISTABLE WITH
CLEAR

TYPICAL CONSTRUCTION
SILICON MONOLITHIC
BIPOLAR TTL-LOW-POWER
SCHOTTKY

refer to Appendix A1.3
Dual-in-Line (ceramic)

ASSESSMENT LEVELS
R, S, T AND V

1. Type description

1.1 Truth table

INPUTS			OUTPUTS
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q ₀

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.1 Truth table (contd)

H = High level

L = Low level

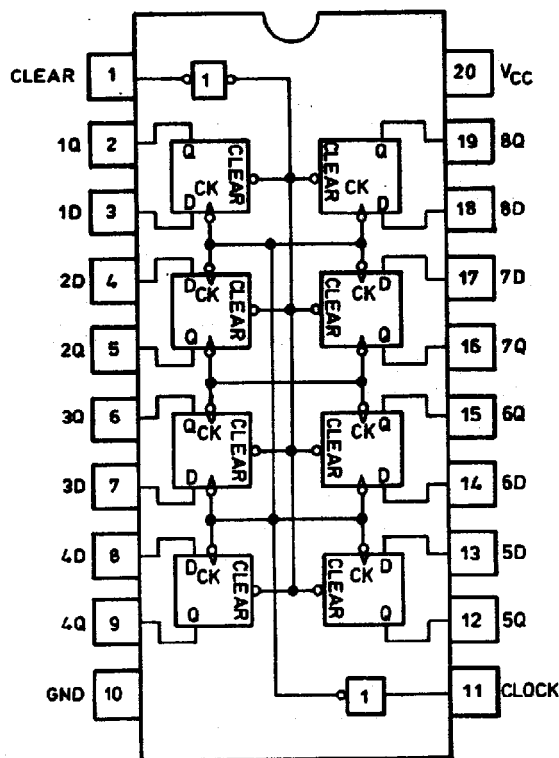
Q_0 = Q output before the indicated steady-level input conditions were established

X = Logic level irrelevant

↑ = Transition from Low to High level

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Octal D-type bistable with clear

1.2.2 Type designation

TEMPERATURE RANGE		PACKAGE		
		Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0	+ 70	74LS273J	N	W
-25	+ 85	84LS273J		
-40	+ 85	64LS273J		
-55	+125	54LS273J		

1.2.3 Marking

Each circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1 Maximum continuous supply voltage V_{CC} -0,5V
+7,0V

2.2 Maximum input voltages

2.2.1 Maximum input voltage V_I -0,5V
+7,0V

2.2.2 Maximum input voltage between multiple emitter transistor inputs V_{II} +5,5V

			54LS	64LS	74LS	84LS
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. -55 max. +125	-40 +85	0 +70	-25 +85

			54LS	64LS	74LS	84LS
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. -65 max. +150	(All types)		

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS	4,5 - 5,5	V
		64/74/84LS	4,75 - 5,25	V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V

3.1 (contd)

Description	Symbol	Type	Value	Unit
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μA
D.C. noise margin				
at Low level ($V_{ILA} - V_{OLA}$)	V_{NL}	All types	0,3	V
at High level ($V_{OHB} - V_{IHB}$)	V_{NH}	54LS 64/74/84LS	0,5 0,7	V V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	All outputs open data and clear inputs = 4,5V Clock 0V then 4,5V	V_{CC} max.	I_{CC}	-	27,0	mA
High level input current	$V_{IH(1)} = 7,0V$ $V_{IH(2)} = 2,7V$	V_{CC} max.	$I_{IH(1)}$	-	0,1	mA
		V_{CC} max.	$I_{IH(2)}$	-	20,0	μA
Low level input current	$V_{IL} = 0,4V$	V_{CC} max.	$-I_{IL}$	-	0,4	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	V_{CC} min.	$-V_{ICA}$	-	1,5	V
Output voltage	$I_{OH} = -400,0\mu A$ $I_{OH} = -400,0\mu A$ All types $I_{OL(1)} = 4,0mA^{(1)}$ 64/74/84LS $I_{OL(2)} = 8,0mA^{(2)}$	V_{CC} min.	V_{OH}	2,5	-	V
			V_{OH}	2,7	-	V
			$V_{OL(1)}$	-	0,4	V
			$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_O = 0V^{(3)}$	V_{CC} max.	$-I_{OS}$	20,0	100,0	mA
Propagation times	$T_{amb} = 25^\circ C^*$ test conditions as in Sub-group A5	5,0V				
All types						
From To						
Clear and Clock			t_{PHL}	-	27,0	ns
Clock	Q		t_{PLH}	-	27,0	ns
Duration of Clock pulse			$t_{p(clock)}$	20,0	-	ns
Duration of Clear pulse			$t_{p(clear)}$	20,0	-	ns
Minimum set-up time	Data input Clear inactive state		t_{set-up}	20,0†	-	ns
				25,0†	-	ns
Maximum clock frequency			$f_{(clock)}$	30,0	-	MHz
Minimum hold time			$t_{(hold)}$	5,0†	-	ns

† with reference to the rising edge of the clock pulse

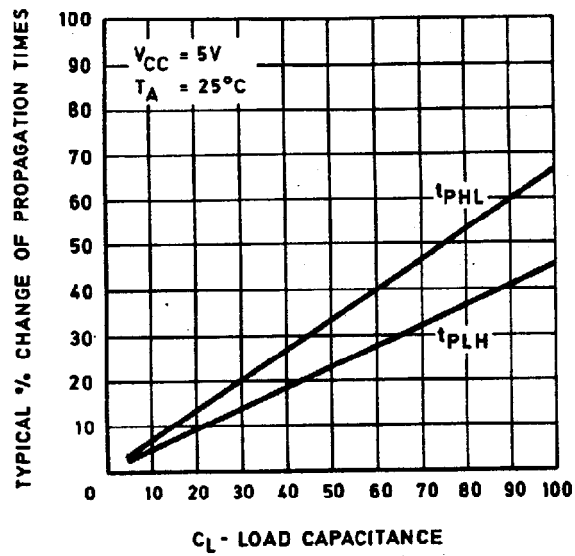
(1) Fan out = 10, (2) Fan out = 20,

(3) Only one output at a time, duration $t \leq 1$ sec

* See 3.2.1 of this specification

3.3 Supplementary information

3.3.1 Change of typical propagation time with output loading



Propagation time Vs. load capacitance

3.3.2 Variation of propagation time with temperature

