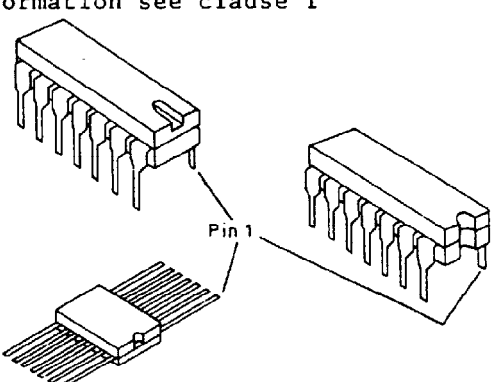


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90103 - 107 ISSUE 1 AUGUST 1981 Page 1 of 20 pages
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS290 64LS290 74LS290 84LS290
Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A50B) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	SEE PD 9002 AND CECC 00 200 For ordering information see clause 1 DECADE DIVIDE-BY-2 AND DIVIDE-BY-5 COUNTERS WITH SUPPLY TO PINS 7 AND 14 TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200 for details of manufacturers approved to this specification

1.1 Truth table (contd)

BCD count sequence
(See note A)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Reset/count truth table

RESET INPUTS				OUTPUT			
R _O (1)	R _O (2)	R _g (1)	R _g (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X				
L	X	X	L				
X	L	L	X				

1.1 Truth table (contd)

Bi-quinary (5-2)
(See note B)

COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

NOTE A) Output Q_A is connected to input B for BCD count

NOTE B) Output Q_D is connected to input A for bi-quinary count

NOTE C) Output Q_A is connected to input B

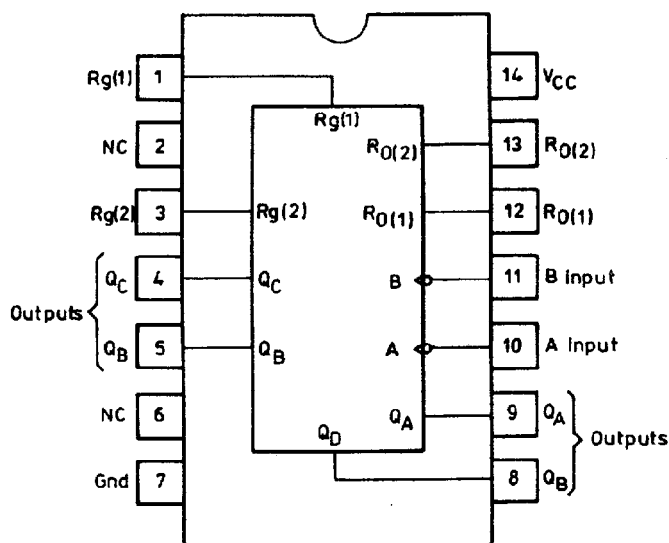
H = High level

L = Low level

X = Logic level irrelevant

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Decade divide-by-2 and divide-by-5
counters with supply to pins 7 and 14

Terminals marked with NC are not connected internally and may be used as electrical support points. The applied voltage shall not exceed 7,0V.

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS290J	N	W
-25 + 85	84LS290J		
-40 + 85	64LS290J		
-55 +125	54LS290J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit typedesignation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}	-0,5V +7,0V				
2.2	Maximum input voltages						
2.2.1	Maximum input voltage	V_I	-0,5V +7,0V (Reset input) +5,5V (A and B inputs)				
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}	+5,5V				
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. -55 max. +125	54LS -40 64LS +85	74LS 0 +70	84LS -25 +85	
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. -65 max. +150	(All types)			

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage Reset inputs A and B inputs	V_{IHB}	All types All types	2,0 2,0	V V
Maximum value of High level input voltage Reset inputs A and B inputs	V_{IHA}	All types All types	7,0 5,5	V V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μ A
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$) at High level ($V_{OHB} - V_{IHB}$)	V_{NL} V_{NH}	All types 54LS 64/74/84LS	0,3 0,5 0,7	V V V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	R_0 inputs 4,5V then grounded, other inputs grounded. Outputs open circuit	V_{CC} max.	I_{CC}	-	15,0	mA
High level input current	$V_{IH(1)} = 7,0V$ Reset input	V_{CC} max.	$I_{IH(1)}$	-	0,1	mA
	$V_{IH(1)} = 5,5V$ A input		$I_{IH(1)}$	-	0,2	mA
	B input		$I_{IH(1)}$	-	0,4	mA
	$V_{IH(2)} = 2,7V$ Reset input		$I_{IH(2)}$	-	20,0	μA
	A input		$I_{IH(2)}$	-	40,0	μA
	B input		$I_{IH(2)}$	-	80,0	μA
Low level input current	$V_{IL} = 0,4V$ Reset input	V_{CC} max.	$-I_{IL}$	-	0,4	mA
	A input		$-I_{IL}$	-	2,4	mA
	B input		$-I_{IL}$	-	3,2	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	V_{CC} min.	$-V_{ICA}$	-	1,5	V
Output voltage	54LS $I_{OH} = -400,0\mu A$	V_{CC} min.	V_{OH}	2,5	-	V
	64/74/84LS $I_{OH} = -400,0\mu A$		V_{OH}	2,7	-	V
	All types $I_{OL(1)} = 4,0mA$ (1)		$V_{OL(1)}$	-	0,4	V
	64/74/84LS $I_{OL(2)} = 8,0mA$ (2)		$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_O = 0V$ or 4,5V (3)	V_{CC} max.	$-I_{OS}$	15,0	130,0	mA

- (1) Fan out = 10, (2) Fan out = 20,
(3) Only one output at a time, duration $t \leq 1$ sec

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Propagation times All types	$T_{amb} = 25^{\circ}C^{*}$ test conditions as in Sub-group A5 <u>From Input</u> <u>To</u> <u>Output</u> A Q_A A Q_D B Q_B B Q_C B Q_D Set-to-0 Any Set-to-9 Q_B, Q_C <u>From Input</u> <u>To</u> <u>Output</u> A Q_A A Q_D B Q_B B Q_C B Q_D Set-to-9 Q_A, Q_D	5,0V	t_{PHL}			
			t_{PHL}	-	18,0	ns
				-	50,0	ns
				-	21,0	ns
				-	35,0	ns
				-	35,0	ns
				-	40,0	ns
				-	40,0	ns
			t_{PLH}	-	16,0	ns
				-	48,0	ns
				-	16,0	ns
				-	32,0	ns
				-	32,0	ns
				-	30,0	ns
Frequency of operation	<u>From Input</u> <u>To</u> <u>Output</u> A Q_A B Q_B		$f_{max.}$	-	32,0	MHz
				-	16,0	MHz
Duration of input count pulse	A input		t_p	15,0	-	ns
	B input		(count)	30,0	-	ns
	Reset input			15,0	-	ns
Reset inactive-level set-up time			t_{su}	25,0	-	ns

*See 3.2.1 of this specification