

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 AND

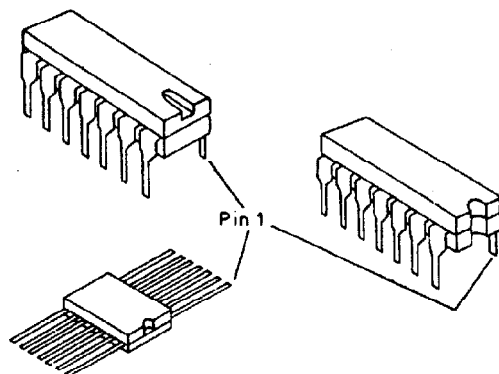
BS CECC 90103 - 108

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**ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:**BS CECC 90 000 : 1976
BS CECC 90 100 : 1977**MANUFACTURERS TYPE NUMBER**54LS293
64LS293
74LS293
84LS293Outline not to scale: Isometric projection
Marking information see clause 1Refer to IEC 191-1-50a (type A50B)
Dual-in-Line (plastic or ceramic)
refer to Appendix A1.3
Flatpack (metal or ceramic)SEE PD 9002 AND CECC 00 200
For ordering information see
clause 1**4-BIT BINARY COUNTER WITH
SUPPLY TO PINS 7 AND 14**TYPICAL CONSTRUCTION
SILICON MONOLITHIC
BIPOLAR TTL-LOW-POWER
SCHOTTKY**ASSESSMENT LEVELS**
R, S, T AND V1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.1 Truth table (contd)

Reset/count truth table

RESET INPUTS		OUTPUT			
R _o (1)	R _o (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

Count sequence

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = High level

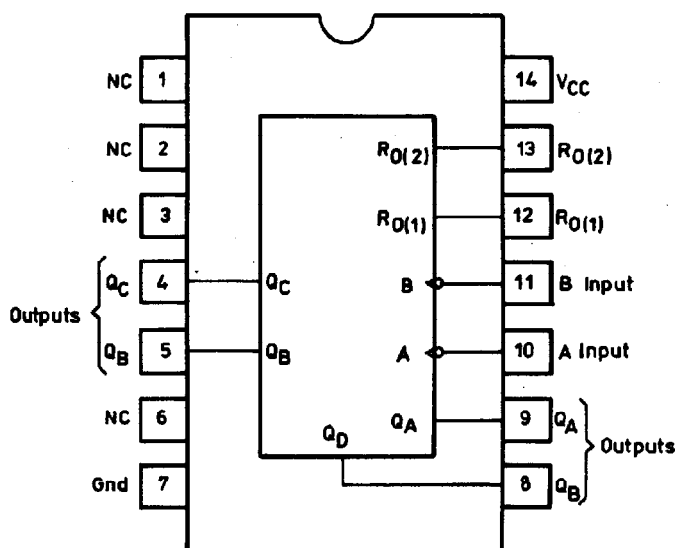
L = Low level

X = Logic level irrelevant

Output Q_A is connected to input B

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



4-bit binary counter with supply to pins 7 and 14

Terminals marked with 'NC' are not connected internally and may be used as electrical support points. The applied voltage shall not exceed 7,0V.

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS 293J	N	W
-25 + 85	84LS 293J		
-40 + 85	64LS 293J		
-55 +125	54LS 293J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information.

1.3 (contd)

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}	-0,5V +7,0V				
2.2	Maximum input voltages						
2.2.1	Maximum input voltage	V_I	-0,5V +7,0V (R input) +5,5V (A and B input)				
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}	+5,5V				
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. max.	54LS -55 +125	64LS -40 +85	74LS 0 +70	84LS -25 +85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. max.	-65 +150	(All types)		

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage Reset inputs A and B inputs	V_{IHB}	All types All types	2,0 2,0	V V
Maximum value of High level input voltage Reset inputs A and B inputs	V_{IHA}	All types All types	7,0 5,0	V V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V

3.1 (contd)

Description	Symbol	Type	Value	Unit
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	$-I_{OHA}$	All types	400,0	μA
DC noise margin at Low level ($V_{ILA} - V_{OLA}$)	V_{NL}	All types	0,3	V
at High level ($V_{OHB} - V_{IHB}$)	V_{NH}	54LS 64/74/84LS	0,5 0,7	V V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	R_O inputs 4,5V then ground, other inputs ground. Outputs open circuit.	V_{CC} max.	I_{CC}	-	15,0	mA

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
High level input current	$V_{IH(1)} = 7,0V$	$V_{CC} \text{ max.}$				
Reset input			$I_{IH(1)}$	-	0,1	mA
A input	$V_{IH(1)} = 5,5V$		$I_{IH(1)}$	-	0,2	mA
B input			$I_{IH(1)}$	-	0,2	mA
Reset input	$V_{IH(2)} = 2,7V$		$I_{IH(2)}$	-	20,0	μA
A input			$I_{IH(2)}$	-	40,0	μA
B input			$I_{IH(2)}$	-	40,0	μA
Low level input current	$V_{IN} = 0,4V$	$V_{CC} \text{ max.}$				
Reset input			$-I_{IL}$	-	0,4	mA
A input			$-I_{IL}$	-	2,4	mA
B input			$-I_{IL}$	-	1,6	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	$V_{CC} \text{ min.}$	$-V_{ICA}$	-	1,5	V
Output voltage	$V_{IN} = 0,4V$ or 2,0V as appropriate	$V_{CC} \text{ min.}$				
54LS			V_{OH}	2,5	-	V
64/74/84LS			V_{OH}	2,7	-	V
All types	$I_{OL} = 4,0mA$ (1)		V_{OL}	-	0,4	V
64/74/84LS	$I_{OL} = 8,0mA$ (2)		V_{OL}	-	0,5	V
Output short circuit current	$V_O = 0V$ (3)	$V_{CC} \text{ max.}$	$-I_{OS}$	15,0	130,0	mA
Propagation times	$T_{amb} = 25^{\circ}C^*$ test conditions as in Sub-group A5	5,0V				
All types						

(1) Fan out = 10, (2) Fan out = 20

(3) Only one output at a time, duration $t \leq 1$ sec

*See 3.2.1 of this specification

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Propagation times (contd)						
<u>From Input</u> <u>To Output</u>			t_{PHL}			
A Q_A				-	18,0	ns
A Q_D				-	70,0	ns
B Q_B				-	21,0	ns
B Q_C				-	35,0	ns
B Q_D				-	51,0	ns
Set-to-0 Any				-	40,0	ns
<u>From Input</u> <u>To Output</u>			t_{PLH}			
A Q_A				-	16,0	ns
A Q_D				-	70,0	ns
B Q_B				-	16,0	ns
B Q_C				-	32,0	ns
B Q_D				-	51,0	ns
Maximum frequency of operation						
<u>From Input</u> <u>To Output</u>			$f_{max.}$			
A Q_A				32,0	-	MHz
B Q_B				16,0	-	MHz
Duration of input count pulse						
	A input		$t_p(COUNT)$	15,0	-	ns
	B input			30,0	-	ns
	Reset input			15,0	-	ns
Reset inactive-level set-up time						
			$t_{(set-up)}$	25,0	-	ns