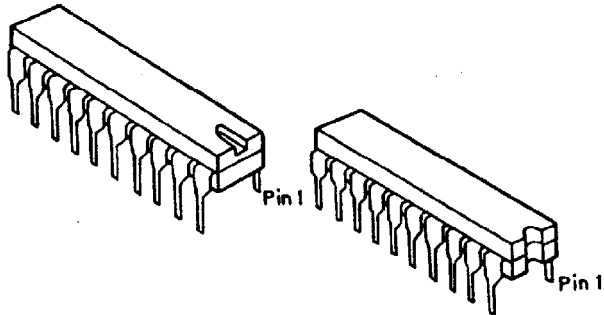


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	BS CECC 90103 - 110 ISSUE 1 NOVEMBER 1981 Page 1 of 24 pages
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS299 64LS299 74LS299 84LS299
Outline not to scale: Isometric projection Marking information see clause 1  refer to Appendix A1.3 Dual-in-Line (ceramic)	SEE PD 9002 AND CECC 00 200 For ordering information see clause 1 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-LEVEL OUTPUTS TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
 for details of manufacturers approved to this specification

1.1 Truth table (contd)

MODE	INPUTS							INPUTS/OUTPUTS								OUTPUTS		
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL		CLOCK	SERIAL		A/Q _A	B/Q _B	C/Q _C	D/Q _D	E/Q _E	F/Q _F	G/Q _G	H/Q _H	Q _A -	Q _H -
		S1	S0	$\overline{G1}+$	$\overline{G2}+$		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q _{AO}	Q _{BO}	Q _{CO}	Q _{DO}	Q _{EO}	Q _{FO}	Q _{GO}	Q _{HO}	Q _{AO}	Q _{HO}
	H	X	X	L	L	L	X	X	Q _{AO}	Q _{BO}	Q _{CO}	Q _{DO}	Q _{EO}	Q _{FO}	Q _{GO}	Q _{HO}	Q _{AO}	Q _{HO}
Shift Right	H	L	H	L	L	↑	X	H	H	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	H	Q _{Cn}
	H	L	H	L	L	↑	X	L	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	L	Q _{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	Q _{Hn}	H	Q _{Bn}	H
	H	H	L	L	L	↑	L	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	Q _{Hn}	L	Q _{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

H = High level

L = Low level

X = Logic level irrelevant

↑ = When one or both controls are High the eight input/output terminals are disabled to the high-impedance level, however, sequential operation or clearing of the register is not affected.

a.....h = The level of the steady level input and inputs A through H, respectively. This data is loaded into the Bistables while the Bistable outputs are isolated from the input/output terminals.

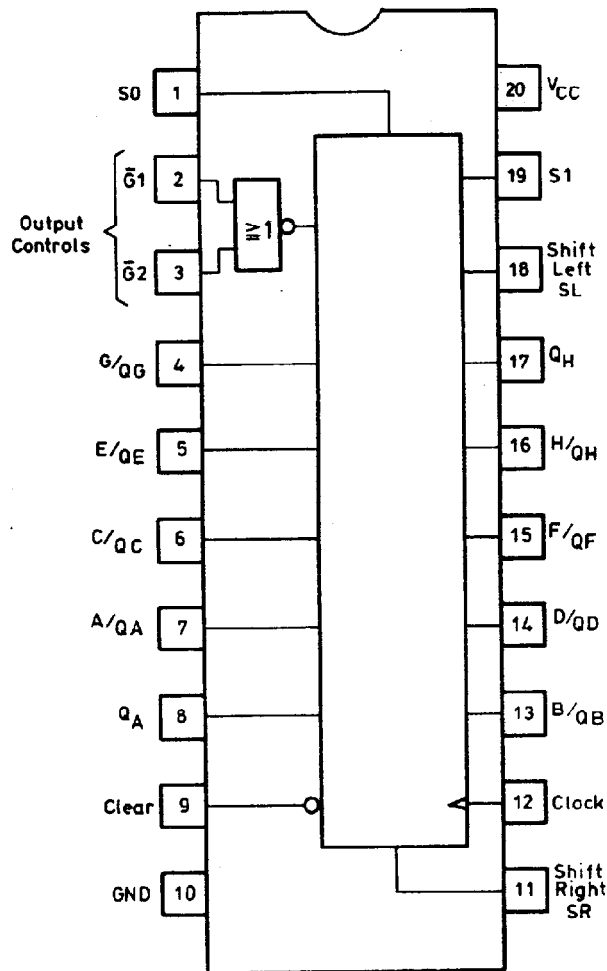
↑ = Low to High transition

Q(A-H)₀ = Level of Q before the indicated steady level input conditions were established.

Q(A-H)₀ = Level of Q before the most recent active transition of the clock pulse is indicated by ↑

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



8-bit universal shift/storage registers with 3 level outputs

Three level device

A device whose output can be driven into the High, Low or high-impedance level.

High-impedance level

That level of a device in which the output acquires a high-impedance characteristic.

High-impedance output leakage current

The current measured at the output terminal with input conditions applied such as to cause the switching element to be in the high-impedance level.

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS229J	N	W
-25 + 85	84LS229J		
-40 + 85	64LS229J		
-55 +125	54LS229J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}	-0,5V +7,0V				
2.2	Maximum input voltages						
2.2.1	Maximum input voltage	V_I	-0,5V (Other inputs) +7,0V (A through H)				
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}	+5,5V				
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. -55 max. +125	64LS -40 84LS +85	74LS 0 +70	84LS -25 +85	
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. -65 max. +150	(All types)			

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output Q_A through Q_H Q_{A^-} and Q_{H^-}	I_{OLA}	All types 64/74/84LS All types 64/74/84LS	12,0 24,0 4,0 8,0	mA mA mA mA
Maximum value of output current for each output at V_{OH} Q_A through Q_H Q_{A^-} and Q_{H^-}	I_{OHA}	All types 64/74/84LS All types	-1,0 -2,6 -0,4	mA mA mA
High impedance level output current (leakage)	I_{OHZ} $-I_{OLZ}$	All types All types	40,0 400,0	μ A μ A
Maximum applied off level voltage	V_{OZA}	All types	5,5	V
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$) at High level ($V_{OHB} - V_{IHB}$)	V_{NL} V_{NH}	All types 54LS 64/74/84LS	0,3 0,5 0,7	V V V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	Inputs grounded outputs open	V_{CC} max.	I_{CC}	-	53,0	mA
High level input current		V_{CC} max.				
S0 and S1	$V_{IH(1)} = 7,0V$		$I_{IH(1)}$	-	0,2	mA
Any other	$V_{IH(1)} = 7,0V$		$I_{IH(1)}$	-	0,1	mA
A through H	$V_{IH(1)} = 5,5V$		$I_{IH(1)}$	-	0,1	mA
S0 and S1	$V_{IH(2)} = 2,7V$		$I_{IH(2)}$	-	40,0	µA
Any other	$V_{IH(2)} = 2,7V$		$I_{IH(2)}$	-	20,0	µA
A through H	$V_{IH(2)} = 2,7V$		$I_{IH(2)}$	-	40,0	µA
Low level input current	$V_{IN} = 0,4V$	V_{CC} max.				
S0 and S1			$-I_{IL}$	-	0,8	mA
Any other			$-I_{IL}$	-	0,4	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	V_{CC} min.	$-V_{ICA}$	-	1,5	V
Output voltage		V_{CC} min.				
All types	$I_{OH} = I_{OHA}$		V_{OH}	2,4	-	V
Q_A through Q_H			V_{OH}	2,5	-	V
Q'_A through Q'_H			V_{OH}	2,7	-	V
54LS			V_{OH}	2,7	-	V
64/74/84LS			V_{OH}	2,7	-	V

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Output voltage (contd)						
All types	$I_{OL} = 12,0mA$ (1)		V_{OL}	-	0,4	V
Q_A through Q_H	$I_{OL} = 24,0mA$ (2)		V_{OL}	-	0,5	V
64/74/84LS						
Q_A through Q_H	$I_{OL} = 4,0mA$ (1)		V_{OL}	-	0,4	V
All types						
Q_A and Q_H	$I_{OL} = 8,0mA$ (2)		V_{OL}	-	0,5	V
64/74/84LS						
Q_A and Q_H						
Output short circuit current	$V_O = 0V$ (3)	$V_{CC} \text{ max.}$	$-I_{OS}$	20,0	130,0	mA
Propagation times	$T_{amb} = 25^\circ C^*$ test conditions as in Sub-group A5	5,0V				
All types						
High to Low level	From To Clock Q_A through Q_H Clear Q_A through Q_H Clock Q_A and Q_H Clear Q_A and Q_H		t_{PHL} t_{PHL} t_{PHL} t_{PHL}	- - - -	39,0 40,0 39,0 40,0	ns ns ns ns
Low to High level	From To Clock Q_A and Q_H Clock Q_A through Q_H		t_{PLH} t_{PLH}	- -	33,0 25,0	ns ns
Output enable time to High level	G_1 and G_2 to Q_A through Q_H		t_{PZH}	-	21,0	ns
Output enable time to Low level	G_1 and G_2 to Q_A through Q_H		t_{PZL}	-	30,0	ns
Output disable time from High level	$C_L = 5,0pF$ G_1 and G_2 to Q_A through Q_H		t_{PHZ}	-	15,0	ns

- (1) Fan out = 30, (2) Fan out = 60,
(3) Only one output at a time, duration $t \leq 1 \text{ sec}$
* See 3.2.1 of this specification

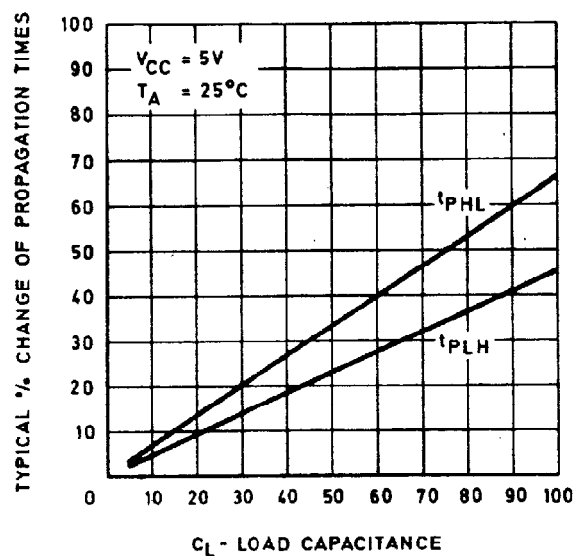
3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Output disable time from Low level	$C_L = 5,0pF$ G_1 and G_2 to Q_A through Q_H		t_{PLZ}	-	15,0	ns
Clock frequency			f_{clock}	-	25,0	MHz
Clock pulse width	Clock High Clock Low		$t_{p(clock)}$	30,0 10,0	- -	ns ns
Clear pulse width			$t_{p(clear)}$	20,0	-	ns
Set-up time			t_{set-up}	35,0†	-	ns
Select			t_{set-up}	20,0†	-	ns
Data			t_{set-up}	20,0†	-	ns
Clear (inactive level)						
Hold time			t_{hold}	10,0†	-	ns
Select			t_{hold}	0†	-	ns
Data						

† = Enabled by the leading edge of the clock pulse

3.3 Supplementary information

3.3.1 Change of typical propagation time with output loading



Propagation time Vs. load capacitance