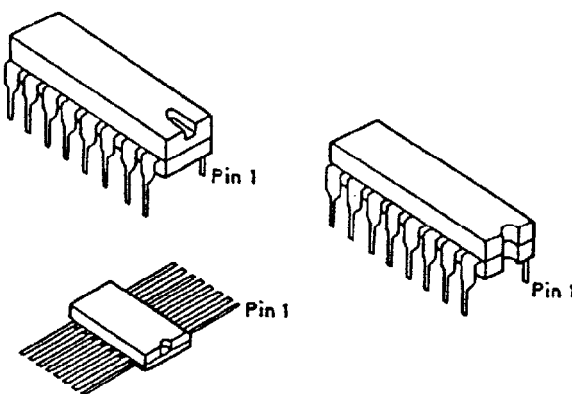


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90103-117 ISSUE 1 JULY 1982
SPECIFICATION AVAILABLE FROM:- As shown in PD 9002 AND CECC 00 200 AND TEXAS INSTRUMENTS LIMITED, MANTON LANE, BEDFORD, MK41 7PA	 Page 1 of 22 Pages
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH:- BS CECC 90 000 : 1982 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS348 64LS348 74LS348 84LS348
Outline not to scale. Isometric projection Marking information see Clause 1  IEC 191-2 (Type A 50 C) Dual-in-line (plastic or ceramic) Appendix A1.3 Flatpack (metal or ceramic)	SEE PD 9002 AND CECC 00 200 For ordering information see Clause 1 DETAIL SPECIFICATION FOR 8-LINE TO 3-LINE OCTAL PRIORITY ENCODERS WITH 3-STATE OUTPUTS TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR ASSESSMENT LEVELS R, S, T AND V

1. TYPE DESCRIPTION

1.1. Truth table (see Page 2)

REFER TO QUALIFIED PRODUCTS LIST PD 9002 AND/OR CECC 00 200
 FOR DETAILS OF MANUFACTURERS APPROVED TO THIS SPECIFICATION

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1.1 Truth table (contd)

INPUTS									OUTPUTS				
E1	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	Z	Z	Z	H	H
L	H	H	H	H	H	H	H	H	Z	Z	Z	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = High level

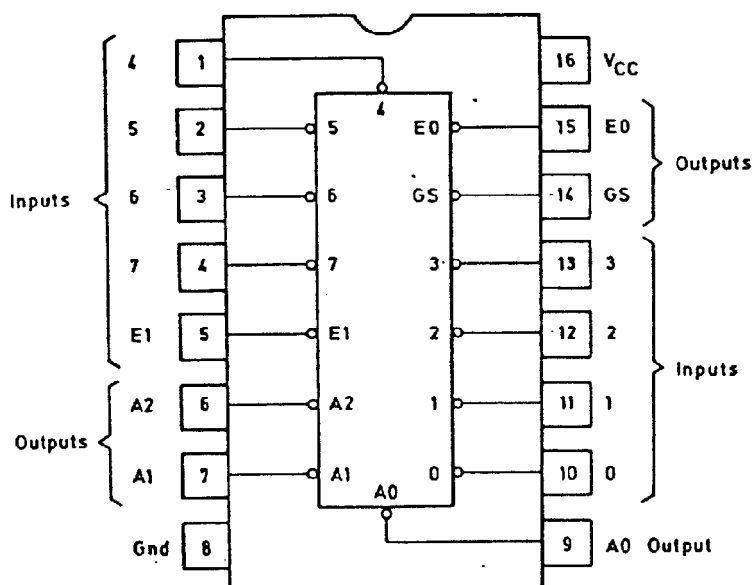
L = Low level

X = Logic level irrelevant

Z = High impedance state

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



8-line to 3-line octal priority encoders

The encoder features priority decoding of the inputs to ensure that only the highest order data line is encoded. The encoders encode eight data lines to three line Binary (octal). Cascading circuitry (enable input E1 and enable output E0) has been provided to allow octal expansion without the need for external circuit. Data inputs and outputs are active at the low level. All inputs are buffered to represent the one normalised TTL low power Schottky load. Outputs A0, A1 and A2 are implemented in three-state logic for easy expansion up to 64 lines.

1.2.2 Type designation

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TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS348J	N	W
-25 + 85	84LS348J		
-40 + 85	64LS348J		
-55 +125	54LS348J		

1.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.4 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1).

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}						-0,5V +7,0V
2.2	Maximum input voltages							
2.2.1	Maximum input voltage	V_I						-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}						+5,5V
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. max.	54LS -55 +125	64LS -40 +85	74LS 0 +70	84LS -25 +85	
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. max.	-65 +150	(All types)			

3. Recommended Operating Conditions and Associated Characteristics (not for inspection purposes)

3.1 Recommended Operating Conditions

These apply over the operating ambient temperature range unless otherwise stated.

DESCRIPTION	SYMBOL	TYPE	VALUE	UNIT
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4.75 - 5.25	V
Minimum value of High level input voltage	V_{IHB}	All Types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All Types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All Types	-0,8	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0.8	V
Maximum value of Low level output current for each output	I_{OLA}	54LS EO, GS AO,A1,A2 64/74/84LS EO, GS AO,A1,A2	4,0 12,0 8.0 24.0	mA mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All Types EO,GS 54LS AO,A1,A2 64/74/84	-400,0 -1.0 -2.6	μ A mA mA

3.2. Associated Characteristics

3.2.1. Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*).

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2.

CHARACTERISTICS	CONDITIONS	$V_{CC}(V)$	SYMBOL	MIN.	MAX.	UNIT
Total supply current per package	Condition 1** Condition 2**	V_{CC} max.	$I_{CC(1)}$ $I_{CC(2)}$	- -	25,0 23,0	mA mA
High level input current						
Inputs 1 through 7	$V_{IH(1)} = 7,0V$	V_{CC} max.	$I_{IH(1)}$	-	0,2	mA
All other inputs				-	0,1	mA
Inputs 1 through 7	$V_{IH(2)} = 2,7V$	V_{CC} max.	$I_{IH(2)}$	-	40,0	μA
All other inputs				-	20,0	μA
Low level input current						
Inputs 1 through 7	$V_{IL} = 0,4V$	V_{CC} max.	$-I_{IL}$	-	0,8	mA
All other inputs				-	0,4	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	V_{CC} min.	$-V_{ICA}$	-	1,5	V
Output voltage						
54 LS AO, A1, A2	$I_{OH} = -1,0mA$	V_{CC} min.	V_{OH}	2,4	-	V
64/74/84LS AO, A1, A2	$I_{OH} = -2,6mA$		V_{OH}	2,4	-	V
54 LS EO, GS	$I_{OH} = -400,0\mu A$		V_{OH}	2,5	-	V
64/74/84LS EO, GS	$I_{OH} = -400,0\mu A$		V_{OH}	2,7	-	V
ALL TYPES AO, A1, A2	$I_{OL} = 12,0mA$		V_{OL}	-	0,4	V
ALL TYPES EO, GS	$I_{OL} = 4,0mA$		V_{OL}	-	0,4	V
64/74/84LS AO, A1, A2	$I_{OL} = 24,0mA$		V_{OL}	-	0,5	V
64/74/84LS EO, GS	$I_{OL} = 8,0mA$		V_{OL}	-	0,5	V
Output short circuit current	$V_O = 0V (3)$	V_{CC} max.				
AO, A1, A2	$V_{IL} = 0V$ or 4,5V		$-I_{OS}$	30,0	130,0	mA
EO, GS			$-I_{OS}$	20,0	100,0	mA

- (1) Fan out = 10, (2) Fan out = 20,
(3) Only one output at a time, duration $t < 1$ sec
* See 3.2.1. of this specification
** See Sub-group A3 for conditions

CHARACTERISTICS	CONDITIONS	$V_{CC}(V)$	SYMBOL	MIN.	MAX.	UNIT
High impedance state output current A0, A1, A2	$V_{IH} = 2V$ $V_O = 2,7V$ $V_O = 2,4V$	$V_{CC} \text{ max.}$	I_{OZ} I_{OZ}	20,0 -20,0	20,0 -20,0	μA μA
Propagation times ALL TYPES	$T_{amb} = 25^\circ C^*$ test conditions as in Subgroup A5					
High to Low level 0 through 7 to A0, A1, or A ₂ (in phase)			t_{PHL}	-	30,0	ns
0 through 7 to A0, A1, or A ₂ (out of phase)			t_{PHL}	-	35,0	ns
0 through 7 to E0 (out of phase)			t_{PHL}	-	40,0	ns
0 through 7 to GS (in phase)			t_{PHL}	-	21,0	ns
E1 to GS (in phase)			t_{PHL}	-	36,0	ns
E1 to E0 (in phase)			t_{PHL}	-	35,0	ns

- (1) Fan out = 10, (2) Fan out = 20,
(3) Only one output at a time, duration $t \leq 1 \text{ sec}$
* See 3.2.1. of this specification
** See Subgroup A3 for conditions

3.2.2. (Cont'd)

CHARACTERISTICS	CONDITIONS	$V_{CC}(V)$	SYMBOL	MIN.	MAX.	UNIT
Propagation times (cont'd)						
Low to High level						
0 through 7 to AO, A1 or A2 (in phase)			t_{PLH}	-	17,0	ns
0 through 7 to AO, A1 or A2 (out of phase)			t_{PLH}	-	30,0	ns
0 through 7 to EO (out of phase)			t_{PLH}	-	18,0	ns
0 through 7 to GS (in phase)			t_{PLH}	-	55,0	ns
E1 to GS (in phase)			t_{PLH}	-	17,0	ns
E1 to EO (in phase)			t_{PLH}	-	21,0	ns
High impedance to High level						
E1 to AO, A1 or A2			t_{PZH}	-	39,0	ns
High impedance to Low level						
E1 to AO, A1 or A2			t_{PZL}	-	41,0	ns
High level to High impedance						
E1 to AO, A1 or A2			t_{PHZ}	-	27,0	ns
Low level to High impedance						
E1 to AO, A1 or A2			t_{PLZ}	-	35,0	ns