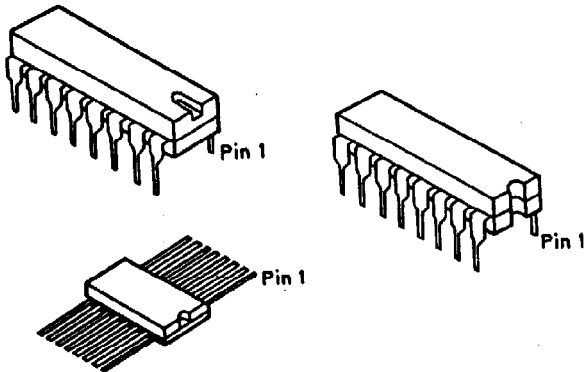


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90103 - 119 ISSUE 1 FEBRUARY 1982 Page 1 of 21 pages
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS353 64LS353 74LS353 84LS353 SEE PD 9002 AND CECC 00 200 For ordering information see clause 1
Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A50C) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	DUAL 4-LINE-TO-1-LINE DATA SELECTOR/MULTIPLEXER WITH INVERTED 3-LEVEL OUTPUTS TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
 for details of manufacturers approved to this specification

1.1 Truth table (contd)

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

H = High level

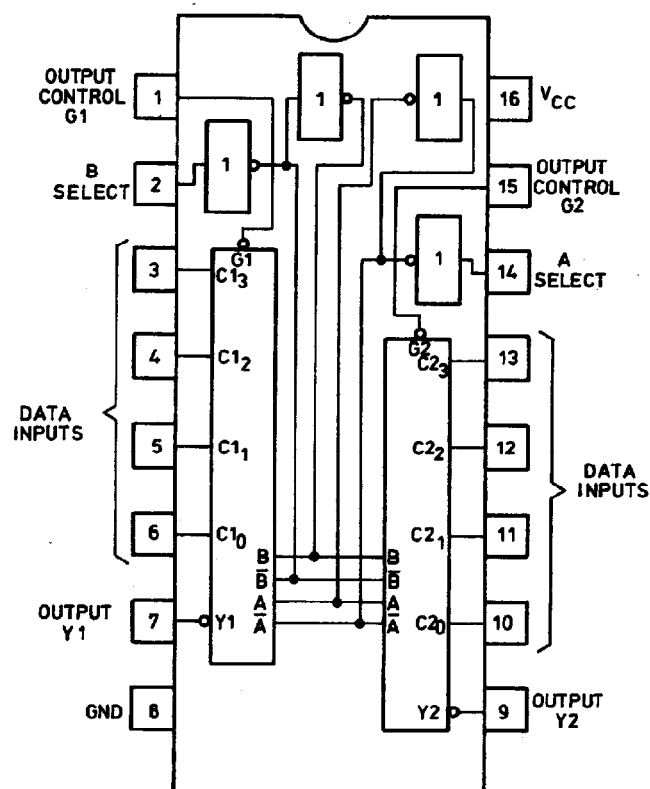
L = Low level

X = Logic level irrelevant

Z = High impedance level (off)

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification

Dual 4-line-to-1-line data selector/
multiplexer with inverted 3-level outputs

1.2.1 (contd)

Three level device

A device whose output can be driven into a High, Low or high-impedance level

High-impedance level

That level of a device in which the output acquires a high-impedance characteristic

High-impedance leakage current

The current measured at the output terminal with input conditions applied such as to cause the switching element to be in the high-impedance level

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS353J	N	W
-25 + 85	84LS353J		
-40 + 85	64LS353J		
-55 +125	54LS353J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}						-0,5V +7,0V
2.2	Maximum input voltages							
2.2.1	Maximum input voltage	V_I						-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}						+5,5V
				54LS	64LS	74LS	84LS	
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. max.	-55 +125	-40 +85	0 +70	-25 +85	
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. max.	-65 +150	(All types)			

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	$-I_{OHA}$	54LS 64/74/84LS	1,0 2,6	mA mA
High impedance level output current (leakage) $V_O = 2,7V$ $V_O = 0,4V$	I_{OHZ} $-I_{OLZ}$	All types All types	20,0 20,0	μA μA

3.1 (contd)

Description	Symbol	Type	Value	Unit
Maximum applied off-level voltage	V_{OZA}	All types	5,5	V
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$)	V_{NL}	All types	0,3	V
at High level ($V_{OHB} - V_{IHB}$)	V_{NH}	54LS 64/74/84LS	0,5 0,7	V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	All inputs grounded Outputs open circuit Enable input = 4,5V Other inputs ground. Outputs open circuit	V_{CC} max.	I_{CC}	-	12,0	mA
			I_{CCZ}	-	14,0	mA

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
High level input current	$V_{IH(1)} = 7,0V$ Enable input = 4,5V	$V_{CC} \text{ max.}$	$I_{IH(1)}$	-	0,1	mA
	$V_{IH(2)} = 2,7V$ Enable input = 4,5V	$V_{CC} \text{ max.}$	$I_{IH(2)}$	-	20,0	μA
Low level input current	$V_{IL} = 0,4V$ Enable input = 0V	$V_{CC} \text{ max.}$	$-I_{IL}$	-	0,4	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	$V_{CC} \text{ min.}$	$-V_{ICA}$	-	1,5	V
Output voltage All types All types 64/74/84LS	$I_{OH} = -I_{OHA} \quad (1)$	$V_{CC} \text{ min.}$	V_{OH}	2,4	-	V
	$I_{OL} = 4,0mA \quad (1)$		V_{OL}	-	0,4	V
	$I_{OL} = 8,0mA \quad (2)$		V_{OL}	-	0,5	V
Output short circuit current	$V_{IN} = 0V \text{ or } 4,5V$ as appropriate† $V_O = 0V \quad (3)$	$V_{CC} \text{ max.}$	$-I_{OS}$	15,0	130,0	mA
Propagation times All types	$T_{amb} = 25^\circ C^*$ test conditions as in Sub-group A5	5,0V				
High to Low level	<u>From</u> <u>To</u>					
	Data Y		t_{PHL}	-	20,0	ns
Low to High level	Select Y		t_{PHL}	-	32,0	ns
	<u>From</u> <u>To</u>					
High-impedance to Low level	Data Y		t_{PLH}	-	25,0	ns
	Select Y		t_{PLH}	-	45,0	ns
High-impedance to High level	From output control to Y		t_{PZL}	-	23,0	ns
Low level to high-impedance	From output control to Y		t_{PZH}	-	23,0	ns
	From output control to Y $C_L = 5pF$		t_{PLZ}	-	27,0	ns

(1) Fan out = 10, (2) Fan out = 20,

(3) Only one output at a time, duration $t \leq 1 \text{ sec}$

*See 3.2.1 of this specification

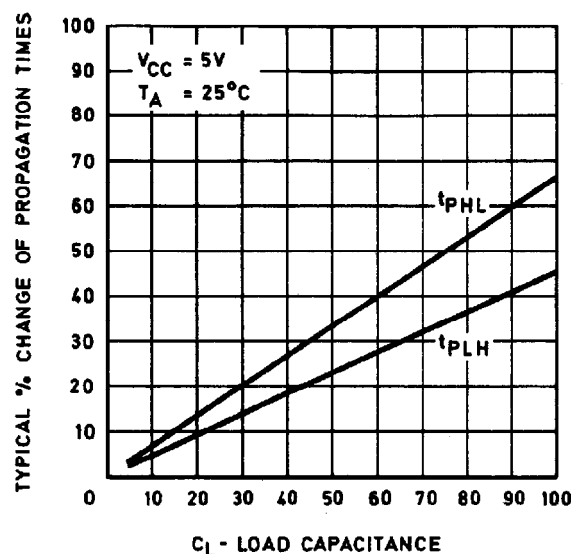
†Refer to truth table

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
High level to high impedance	From output control to Y $C_L = 5,0pF$		t_{PHZ}	-	41,0	ns

3.3 Supplementary information

3.3.1 Change of typical propagation time with output loading



Propagation times Vs. load capacitance