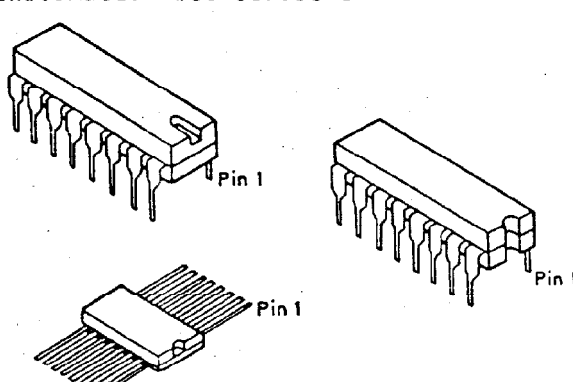


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	BS CECC 90103 - 121 ISSUE 1 NOVEMBER 1981  Page 1 of 20 pages
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS367A 64LS367A 74LS367A 84LS367A
Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A50G) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	SEE PD 9002 AND CECC 00 200 For ordering information see clause 1 NON-INVERTING HEX BUFFERS 2-LINE AND 4-LINE ENABLE INPUTS 3-LEVEL OUTPUTS TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table

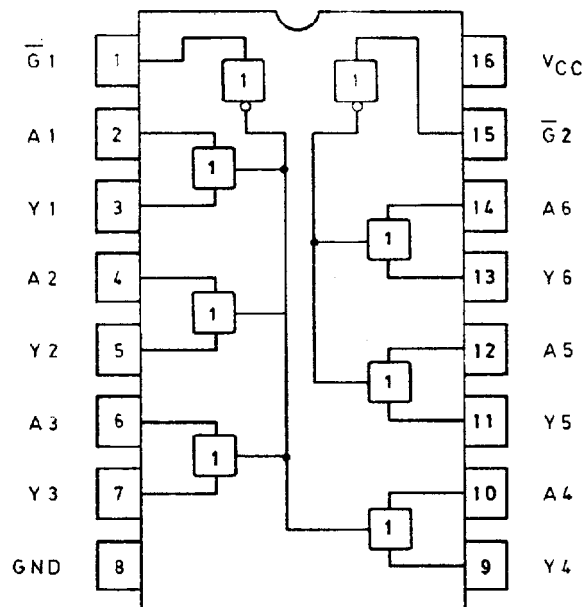
INPUTS		OUTPUTS
$\overline{G}$	A	Y
H	X	Z
L	H	H
L	L	L

H = High level
L = Low level
X = Logic level irrelevant
Z = High impedance level

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Non inverting hex buffers 2-line and
4-line enable inputs 3-level outputs

Three level device

A device whose output can be driven into a High, Low or high impedance level

High impedance level

That level of a device in which the output acquires a high impedance characteristic

High impedance leakage current

The current measured at the output terminal with input conditions applied such as to cause the switching element to be in the high impedance level

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS367AJ	N	W
-25 + 85	84LS367AJ		
-40 + 85	64LS367AJ		
-55 +125	54LS367AJ		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}					-0,5V +7,0V
2.2	Maximum input voltages						-0,5V +7,0V
2.2.1	Maximum input voltage	V_I					+5,5V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}					
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. max.	-55 +125	-40 +85	0 +70	-25 +85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. max.	-65 +150	(All types)		

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	12,0 24,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	54LS 64/74/84LS	-1,0 -2,6	mA mA
Maximum applied off level voltage	V_{OZA}	All types	5,5V	V
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$)	V_{NL}	All types	0,3	V
at High level ($V_{OHB} - V_{IHB}$)	V_{NH}	54LS 64/74/84LS	0,5 0,7	V V

3.2 Associated characteristics

- 3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

3.2.1(contd)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	$V_{IN} = 4,5V$ to control inputs $V_{IN} = 0V$ to all other inputs. Outputs open	V_{CC} max.	I_{CC}	-	28,0	mA
High level input current	$V_{IH(1)} = 7,0V$ $V_{IH(2)} = 2,7V$	V_{CC} max.	$I_{IH(1)}$	-	0,1	mA
		V_{CC} max.	$I_{IH(2)}$	-	20,0	mA
Low level input current	$V_{IN} = 0,4V^*$ Outputs disabled Outputs enabled	V_{CC} max.	$-I_{IL}$	-	20,0	μA
		V_{CC} max.	$-I_{IL}$	-	0,4	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	V_{CC} min.	$-V_{ICA}$	-	1,5	V
Output voltage All types All types 64/74/84LS	$I_{OH} = -I_{OHA}$ $I_{OL(1)} = 12,0mA$ (1) $I_{OL(2)} = 24,0mA$ (2)	V_{CC} min.	V_{OH}	2,4	-	V
			$V_{OL(1)}$	-	0,4	V
			$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_{IN} = 0V$ or $4,5V$ as appropriate† $V_O = 0V$ or $4,5V$ (3)	V_{CC} max.	$-I_{OS}$	30,0	225,0	mA
High impedance level output (leakage) current	$V_O = 0,4V$ $V_O = 2,4V$	V_{CC} max.	I_{OLZ}	-	20,0	μA
			I_{OHZ}	-	20,0	μA

(1) Fan out = 30, (2) Fan out = 60,

(3) Only one output at a time, duration $t \leq 1$ sec

*See 3.2.1 of this specification

†Refer to truth table

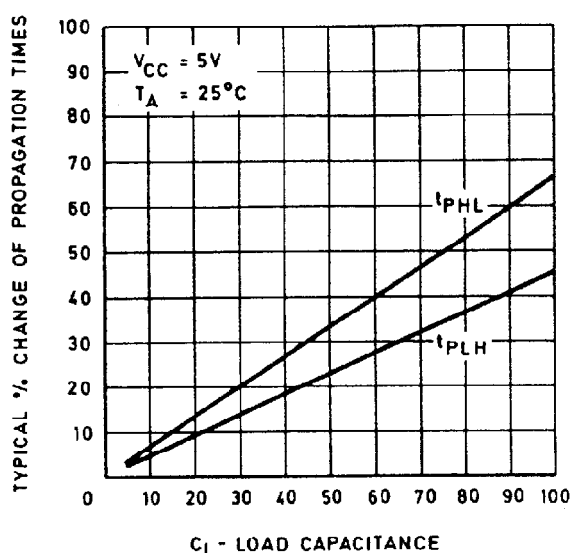
3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Propagation times All types	$T_{amb} = 25^{\circ}C$ test conditions as in Sub-group A5	5,0V				
Low to High level			t_{PLH}	-	16,0	ns
High to Low level			t_{PHL}	-	22,0	ns
High impedance to High level (output enable)			t_{PZH}	-	35,0	ns
High impedance to Low level (output enable)			t_{PZL}	-	40,0	ns
High level to high impedance (output disable)	$C_L = 5,0pF$		t_{PHZ}	-	30,0	ns
Low level to high impedance (output disable)	$C_L = 5,0pF$		t_{PLZ}	-	35,0	ns

*See 3.2.1 of this specification

3.3 Supplementary information

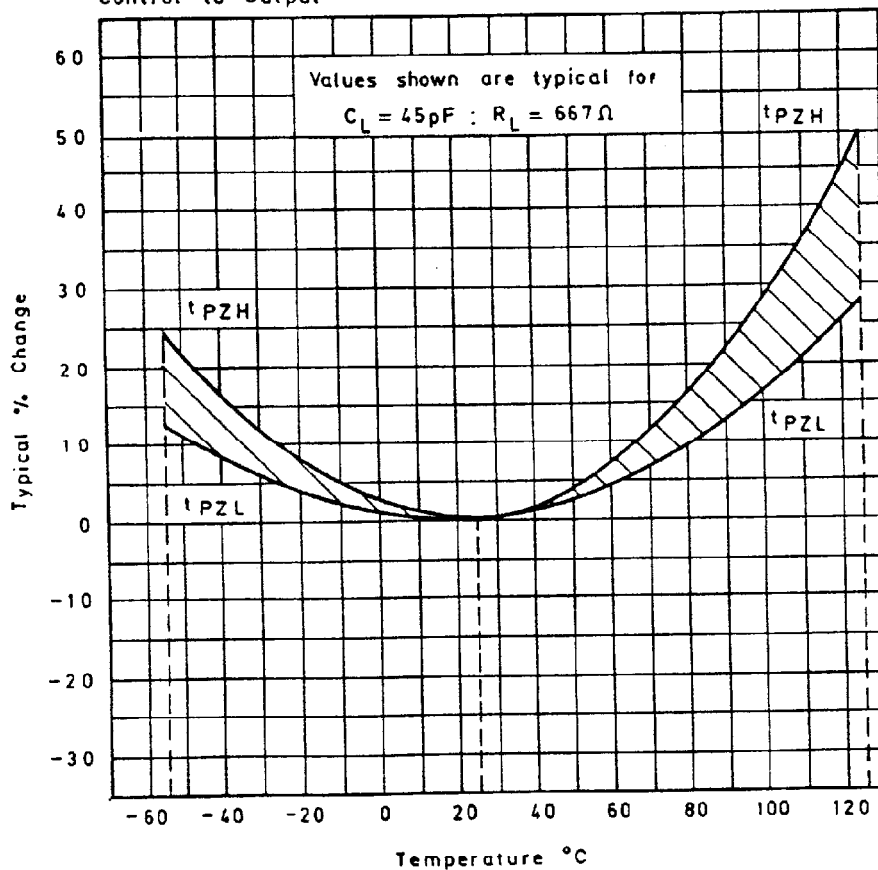
3.3.1 Change of typical propagation time with output loading



Propagation times Vs. load capacitance

3.3.2 Variation of propagation time with temperature

Control to Output



Control to Output

