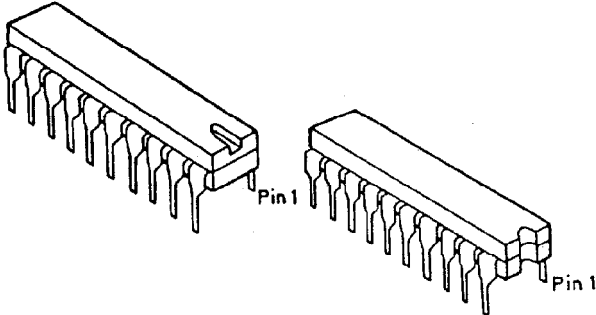


|                                                                                                                                                                                                                                                |                                                                                                                                                                              |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>BRITISH STANDARDS INSTITUTION</b><br>2 PARK STREET, LONDON. W1A 2BS                                                                                                                                                                         | BS CECC 90103 - 122<br><br>ISSUE 1<br><br>NOVEMBER 1981<br><br><br><br>Page 1 of 22 pages |
| Specification available from:- AS SHOWN IN PD 9002<br>AND CECC 00 200 AND                                                                                                                                                                      |                                                                                                                                                                              |
| <b>ELECTRONIC COMPONENTS OF ASSESSED QUALITY</b><br><b>DETAIL SPECIFICATION IN ACCORDANCE WITH:</b><br><br>BS CECC 90 000 : 1976<br>BS CECC 90 100 : 1977                                                                                      | <b>MANUFACTURERS TYPE NUMBER</b><br><br>54LS373<br>64LS373<br>74LS373<br>84LS373                                                                                             |
| <b>Outline not to scale: Isometric projection</b><br><b>Marking information see clause 1</b><br><br><br><br>refer to Appendix A1.3<br>Dual-in-Line (ceramic) | SEE PD 9002 AND CECC 00 200<br>For ordering information see<br>clause 1                                                                                                      |
|                                                                                                                                                                                                                                                | <b>OCTAL D-TYPE LATCHES WITH</b><br><b>3 LEVEL OUTPUTS</b>                                                                                                                   |
|                                                                                                                                                                                                                                                | <b>TYPICAL CONSTRUCTION</b><br>SILICON MONOLITHIC<br>BIPOLAR TTL-LOW-POWER<br>SCHOTTKY<br><br><b>ASSESSMENT LEVELS</b><br>R, S, T AND V                                      |

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200  
 for details of manufacturers approved to this specification

## 1.1 Truth table (contd)

| OUTPUT<br>CONTROL | ENABLE<br>G | D | OUTPUT<br>Q |
|-------------------|-------------|---|-------------|
| L                 | H           | H | H           |
| L                 | H           | L | L           |
| L                 | L           | X | $Q_0$       |
| H                 | X           | X | Z           |

H = High level

L = Low level

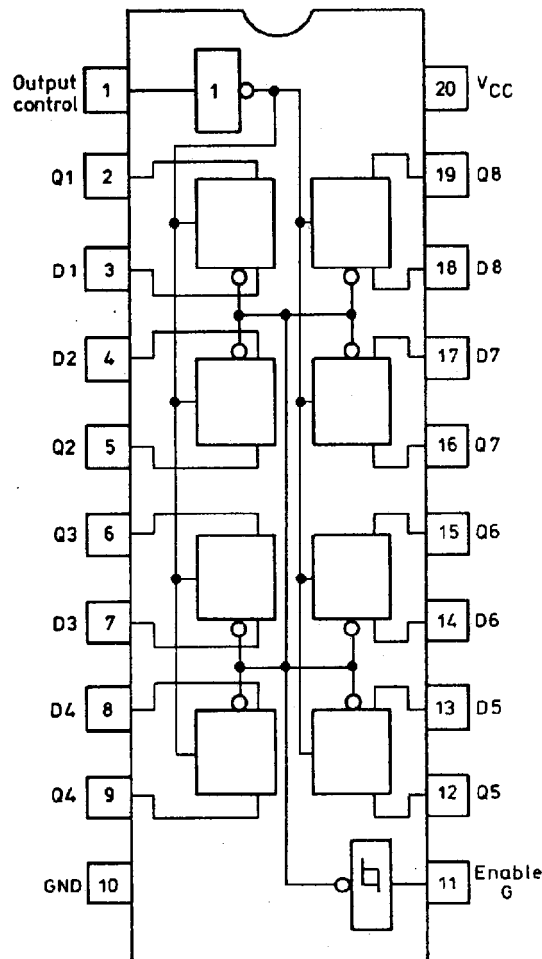
X = Logic level irrelevant

Z = High impedance level

$Q_0$  = Level of Q before the indicated steady level conditions were established

## 1.2 Terminal identification, type designation and marking

### 1.2.1 Terminal identification



Octal D-type latches with  
three level outputs

## 1.2.1 (contd)

## Three level device

A device whose output can be driven into the High, Low or high impedance level

## High impedance level

That level of a device in which the output acquires a high impedance characteristic

## High impedance output leakage current

The current measured at the output terminal with input conditions applied such as to cause the switching element to be in the high impedance level

## 1.2.2 Type designation

| TEMPERATURE RANGE | PACKAGE              |                      |
|-------------------|----------------------|----------------------|
|                   | Ceramic Dual-in-Line | Plastic Dual-in-Line |
| 0 + 70            | 74LS373J             | N                    |
| -25 + 85          | 84LS373J             |                      |
| -40 + 85          | 64LS373J             |                      |
| -55 +125          | 54LS373J             |                      |

## 1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

## 1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

- |       |                                   |          |                |
|-------|-----------------------------------|----------|----------------|
| 2.1   | Maximum continuous supply voltage | $V_{CC}$ | -0,5V<br>+7,0V |
| 2.2   | Maximum input voltages            |          |                |
| 2.2.1 | Maximum input voltage             | $V_I$    | -0,5V<br>+7,0V |

2.2.2 Maximum input voltage between multiple emitter transistor inputs

 $V_{II}$ 

+5,5V

|     |                                                    |                      | 54LS                  | 64LS        | 74LS     | 84LS       |
|-----|----------------------------------------------------|----------------------|-----------------------|-------------|----------|------------|
| 2.3 | Minimum and maximum operating ambient temperatures | $T_{amb}(^{\circ}C)$ | min. -55<br>max. +125 | -40<br>+85  | 0<br>+70 | -25<br>+85 |
| 2.4 | Minimum and maximum storage temperatures           | $T_{stg}(^{\circ}C)$ | min. -65<br>max. +150 | (All types) |          |            |

### 3. Recommended operating conditions and associated characteristics (not for inspection purposes)

#### 3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

| Description                                                                                        | Symbol                  | Type                            | Value                    | Unit               |
|----------------------------------------------------------------------------------------------------|-------------------------|---------------------------------|--------------------------|--------------------|
| Positive supply voltage range                                                                      | $V_{CC}$                | 54LS<br>64/74/84LS              | 4,5 - 5,5<br>4,75 - 5,25 | V<br>V             |
| Minimum value of High level input voltage                                                          | $V_{IHB}$               | All types                       | 2,0                      | V                  |
| Maximum value of High level input voltage                                                          | $V_{IHA}$               | All types                       | 5,5                      | V                  |
| Minimum value of Low level input voltage                                                           | $V_{ILB}$               | All types                       | -0,3                     | V                  |
| Maximum value of Low level input voltage                                                           | $V_{ILA}$               | 54LS<br>64/74/84LS              | 0,7<br>0,8               | V<br>V             |
| Maximum applied "off" level voltage                                                                | $V_{OZA}$               | All types                       | 5,5                      | V                  |
| Maximum value of Low level output current for each output                                          | $I_{OLA}$               | 54LS<br>64/74/84LS              | 12,0<br>24,0             | mA<br>mA           |
| Maximum value of output current for each output at $V_{OH}$                                        | $I_{OHA}$               | 54LS<br>64/74/84LS              | -1,0<br>-2,6             | mA<br>mA           |
| High impedance level output current (leakage)<br>$V_O = 2,4V$<br>$V_O = 0,4V$                      | $I_{OHZ}$<br>$-I_{OLZ}$ | All types<br>All types          | 20,0<br>20,0             | $\mu A$<br>$\mu A$ |
| D.C. noise margin<br>at Low level ( $V_{ILA} - V_{OLA}$ )<br>at High level ( $V_{OHB} - V_{IHB}$ ) | $V_{NL}$<br>$V_{NH}$    | All types<br>54LS<br>64/74/84LS | 0,3<br>0,5<br>0,7        | V<br>V<br>V        |

### 3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (\*)

|                       | 54LS | 64LS | 74LS | 84LS |    |
|-----------------------|------|------|------|------|----|
| T <sub>amb</sub> min. | -55  | -40  | 0    | -25  | °C |
| T <sub>amb</sub> max. | +125 | +85  | +70  | +85  |    |
| V <sub>CC</sub> min.  | 4,5  | 4,75 |      |      | V  |
| V <sub>CC</sub> max.  | 5,5  | 5,25 |      |      |    |

### 3.2.2

| Characteristics                  | Conditions                                                                                                 | $V_{CC}(V)$   | Symbol      | Min. | Max.  | Unit |
|----------------------------------|------------------------------------------------------------------------------------------------------------|---------------|-------------|------|-------|------|
| Total supply current per package | $V_{IL} = 4,5V$ to control input<br>Outputs open                                                           | $V_{CC}$ max. | $I_{CC}$    | -    | 40,0  | mA   |
| High level input current         | $V_{IH(1)} = 7,0V$<br>$V_{IH(2)} = 2,4V$                                                                   | $V_{CC}$ max. | $I_{IH(1)}$ | -    | 0,1   | mA   |
|                                  |                                                                                                            | $V_{CC}$ max. | $I_{IH(2)}$ | -    | 20,0  | μA   |
| Low level input current          | $V_{IN} = 0,4V$ to each input in turn, other inputs at 4,5V                                                | $V_{CC}$ max. | $-I_{IL}$   | -    | 0,4   | mA   |
| Input clamping voltage           | $-I_{IC} = 18,0mA$                                                                                         | $V_{CC}$ min. | $-V_{ICA}$  | -    | 1,5   | V    |
| Output voltage                   | All types $I_{OH} = -I_{OHA}$<br>All types $I_{OL(1)} = 12,0mA$ (1)<br>64/74/84LS $I_{OL(2)} = 24,0mA$ (2) | $V_{CC}$ min. | $V_{OH}$    | 2,4  | -     | V    |
|                                  |                                                                                                            |               | $V_{OL(1)}$ | -    | 0,4   | V    |
|                                  |                                                                                                            |               | $V_{OL(2)}$ | -    | 0,5   | V    |
|                                  |                                                                                                            |               |             |      |       |      |
| Output short circuit current     | $V_{IN} = 0V$ or 4,5V as appropriate<br>$V_O = 0V$ (3)                                                     | $V_{CC}$ max. | $-I_{OS}$   | 15,0 | 130,0 | mA   |

- (1) Fan out = 30, (2) Fan out = 60,  
(3) Only one output at a time, duration  $t \leq 1$  sec

## 3.2.2

| Characteristics                               | Conditions                                                                                                | $V_{CC}(V)$ | Symbol                           | Min.   | Max.           | Unit     |
|-----------------------------------------------|-----------------------------------------------------------------------------------------------------------|-------------|----------------------------------|--------|----------------|----------|
| Propagation times<br>All types                | $T_{amb} = 25^{\circ}C$<br>test conditions as<br>in Sub-group A5                                          | 5,0V        |                                  |        |                |          |
| Low to High level                             | From                      To<br>Data                      Q<br>Clock and                      Q<br>Enable |             | $t_{PLH}$<br>$t_{PLH}$           | -<br>- | 18,0<br>30,0   | ns<br>ns |
| High to Low level                             | From                      To<br>Data                      Q<br>Clock and                      Q<br>Enable |             | $t_{PHL}$<br>$t_{PHL}$           | -<br>- | 18,0<br>30,0   | ns<br>ns |
| High impedance to High level (output enable)  |                                                                                                           |             | $t_{PZH}$                        | -      | 28,0           | ns       |
| High impedance to Low level (output enable)   |                                                                                                           |             | $t_{PZL}$                        | -      | 36,0           | ns       |
| High level to high impedance (output disable) | $C_L = 5pF$                                                                                               |             | $t_{PHZ}$                        | -      | 20,0           | ns       |
| Low level to high impedance (output disable)  | $C_L = 5pF$                                                                                               |             | $t_{PLZ}$                        | -      | 25,0           | ns       |
| Data set-up time<br>54LS<br>64/74/84LS        |                                                                                                           |             | $t_{(set-up)}$<br>$t_{(set-up)}$ | -<br>- | 5,0+<br>5,0+   | ns<br>ns |
| Data hold times<br>54LS<br>64/74/84LS         |                                                                                                           |             | $t_{(hold)}$<br>$t_{(hold)}$     | -<br>- | 20,0+<br>20,0+ | ns<br>ns |

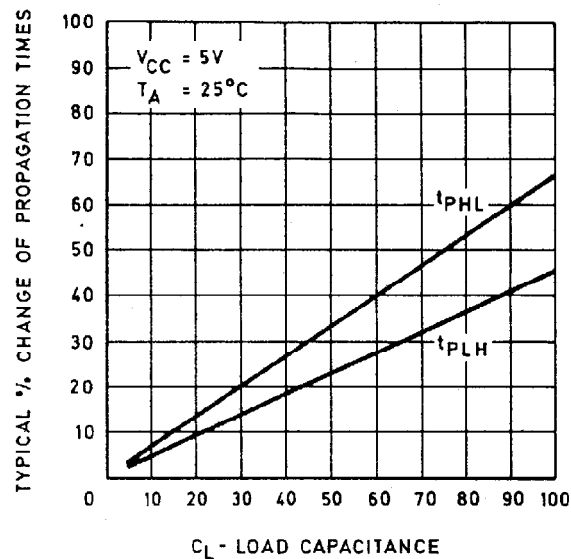
†‡The arrow indicates the transition of the clock/enable input used for reference:

† for the Low to High, ‡ for the High to Low transition

\*See 3.2.1 of this specification

## 3.3 Supplementary information

### 3.3.1 Change of typical propagation time with output loading



Propagation time Vs. load capacitance

### 3.3.2 Variation of propagation time with temperature

