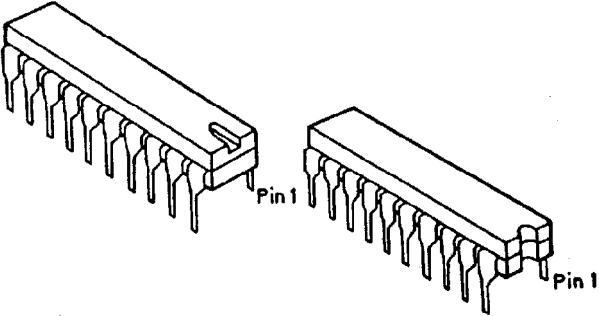


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90103 - 123 ISSUE 1 NOVEMBER 1981  Page 1 of 21 pages	Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977		Outline not to scale: Isometric projection Marking information see clause 1
 refer to Appendix A1.3 Dual-in-Line (ceramic)	MANUFACTURERS TYPE NUMBER 54LS374 64LS374 74LS374 84LS374	SEE PD 9002 AND CECC 00 200 For ordering information see clause 1
	OCTAL D-TYPE EDGE-TRIGGERED BISTABLE CIRCUITS WITH THREE LEVEL OUTPUTS	TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY
	ASSESSMENT LEVELS R, S, T AND V	

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
 for details of manufacturers approved to this specification

1.1 Truth table (contd)

OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

H = High level

L = Low level

X = Logic level irrelevant

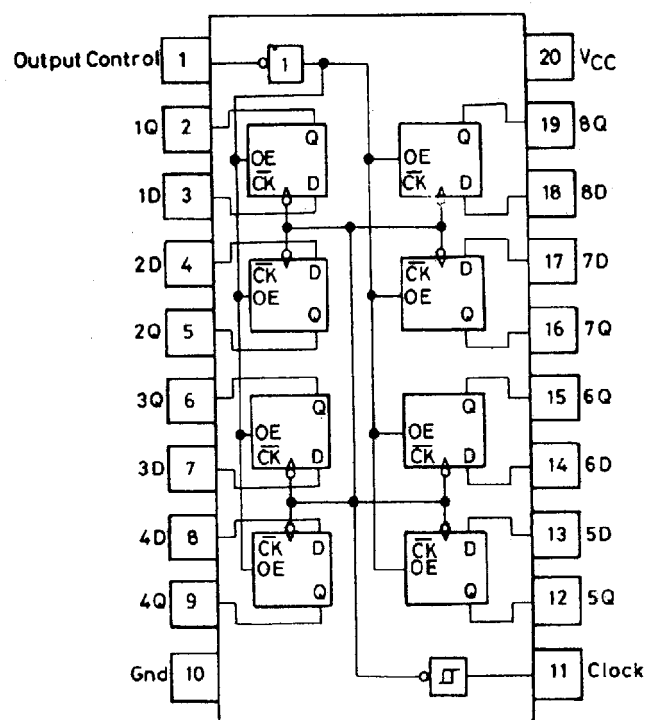
Z = High impedance level (output disabled) see note a

↑ = Transition from Low to High level

Q₀ = Level of Q before the indicated steady-level input conditions were established

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Octal D-type edge-triggered bistable circuits with three level outputs

1.2.1 (contd)

Three level device

A device whose output can be driven into a High, Low or high impedance level.

High impedance level

That level of a device in which the output acquires a high impedance characteristic.

High impedance leakage current

The current measured at the output terminal with input conditions applied such as to cause the switching element to be in the high impedance level.

Note a: The eight bistables of the LS374 bistables are edge-triggered D-type bistables on the positive transition of the clock, the Q outputs will be set to the logic levels that were set up at the D inputs.

The output control does not affect the internal operation of the latches or bistable. That is, the old data can be retained or new data can be entered even when the outputs are off.

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS374J	N	W
-25 + 85	84LS374J		
-40 + 85	64LS374J		
-55 +125	54LS374J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}	-0,5V +7,0V
2.2	Maximum input voltages		
2.2.1	Maximum input voltage	V_I	-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}	+5,5V
			54LS 64LS 74LS 84LS
2.3	Minimum and maximum operating temperatures	$T_{amb}(^{\circ}C)$	min. -55 -40 0 -25 max. +125 +85 +70 +85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. -65 max. +150 (All types)

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	12,0 24,0	V V
Maximum value of output current for each output at V_{OH}	I_{OHA}	54LS 64/74/84LS	1,0 2,6	mA mA
High impedance level output current $V_O = 2,7V$ $V_O = 0,4V$	I_{OHZ} $-I_{OLZ}$	All types All types	20,0 20,0	μA μA

3.1 (contd)

Description	Symbol	Type	Value	Unit
Maximum applied off-level voltage	V_{OZA}	All types	5,5	V
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$)	V_{NL}	All types	0,3	V
at High level ($V_{OHB} - V_{IHB}$)	V_{NH}	54LS 64/74/84LS	0,5 0,7	V V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	$V_{IN} = 4,5V$ to output control inputs Data inputs at 0V Outputs open	V_{CC} max.	I_{CC}	-	50,0	mA
High level input current	$V_{IH(1)} = 7,0V$	V_{CC} max.	$I_{IH(1)}$	-	0,1	mA
	$V_{IH(2)} = 2,7V$	V_{CC} max.	$I_{IH(2)}$	-	20,0	µA
Low level input current	$V_{IL} = 0,4V$	V_{CC} max.	$-I_{IL}$	-	0,4	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	V_{CC} min.	$-V_{ICA}$	-	1,5	V

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Output voltage		$V_{CC} \text{ min.}$				
All types	$-I_{OH} = -I_{OHA}^*$		V_{OH}	2,4	-	V
All types	$I_{OL(1)} = 12,0\text{mA}$ (1)		$V_{OL(1)}$	-	0,4	V
64/74/84LS	$I_{OL(2)} = 24,0\text{mA}$ (2)		$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_{IN} = 0V \text{ or } V_{CC} \text{ max.}$ $V_O = 0V \text{ or } 4,5V$ (3)	$V_{CC} \text{ max.}$	$-I_{OS}$	15,0	130,0	mA
Propagation times	$T_{amb} = 25^\circ C^*$ test conditions as in Sub-group A5	5,0V				
All types			t_{PLH}	-	28,0	ns
			t_{PHL}	-	28,0	ns
Output enable to High level			t_{PZH}	-	28,0	ns
Output enable to Low level			t_{PZL}	-	28,0	ns
Output disable from High level	$C_L = 5\text{pF}$		t_{PHZ}	-	20,0	ns
Output disable from Low level	$C_L = 5\text{pF}$		t_{PLZ}	-	25,0	ns
Maximum clock frequency			f_{clock}	35,0	-	MHz
Maximum duration of clock pulse			$t_{p(\text{clock})}$	15,0	-	ns
Minimum data set-up time			$t_{\text{set-up}}$	20,0 $\uparrow$	-	ns
Minimum data hold time			t_{hold}	0 $\uparrow$	-	ns

(1) Fan out = 10, (2) Fan out = 20,

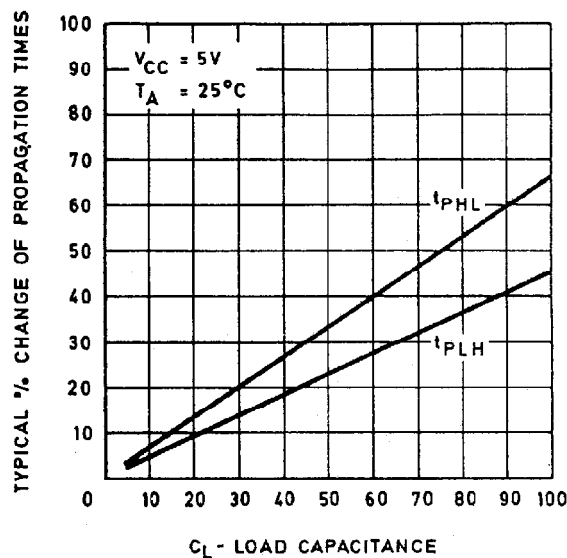
(3) Only one output at a time, duration $t \leq 1 \text{ sec}$

*See 3.1 of this specification

 $\uparrow$ With reference to leading edge of clock pulse

3.3 Supplementary information

3.3.1 Change of typical propagation time with output loading



Propagation times Vs. load capacitance

3.3.2 Variation of propagation time with temperature

