

BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90103 - 126 ISSUE 1 NOVEMBER 1981 Page 1 of 19 pages
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	 MANUFACTURERS TYPE NUMBER 54LS379 64LS379 74LS379 84LS379 SEE PD 9002 AND CECC 00 200 For ordering information see clause 1
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977 Outline not to scale: Isometric projection Marking information see clause 1 Refer to IEC 191-1-50a (type A50B) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	QUAD D-TYPE BISTABLE TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
 for details of manufacturers approved to this specification

1.1 Truth table (contd)

INPUTS			OUTPUTS	
$\overline{G}$	CLOCK	DATA	Q	$\overline{Q}$
H	X	X	Q_0	$\overline{Q}_0$
L	↑	H	H	L
L	↑	L	L	H
X	L	X	Q_0	$\overline{Q}_0$

H = High level

L = Low level

X = Logic level irrelevant

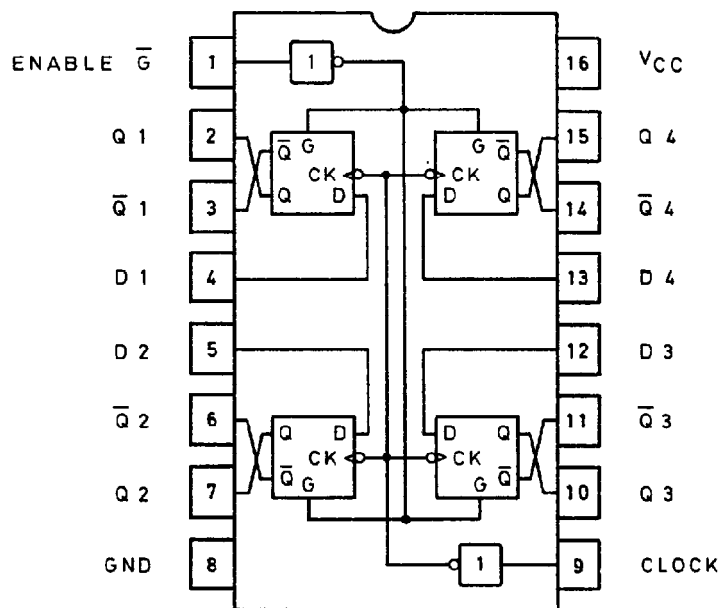
↑ = Low to High transition

Q_0 = The level of Q before the indicated steady level input conditions were established

$\overline{Q}_0$ = Complement of Q_0

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Quad D-type bistable

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS379J	N	W
-25 + 85	84LS379J		
-40 + 85	64LS379J		
-55 +125	54LS379J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}	-0,5V +7,0V
2.2	Maximum input voltages		
2.2.1	Maximum input voltage	V_I	-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}	+5,5V

54LS 64LS 74LS 84LS

2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min.	-55	-40	0	-25
			max.	+125	+85	+70	+85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min.	-65	(All types)		
			max.	+150			

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μA
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$) at High level ($V_{OHB} - V_{IHB}$)	V_{NL} V_{NH}	All types 54LS 64/74/84LS	0,3 0,5 0,7	V V V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	V _{CC} (V)	Symbol	Min.	Max.	Unit
Total supply current per package	All outputs open circuit. Enable/Data inputs grounded. Clock grounded, then 4,5V	V _{CC} max.	I _{CC}	-	15,0	mA
High level input current	V _{IH} (1) = 7,0V	V _{CC} max.	I _{IH} (1)	-	0,1	mA
	V _{IH} (2) = 2,7V	V _{CC} max.	I _{IH} (2)	-	20,0	µA
Low level input current	V _{IL} = 0,4V*	V _{CC} max.	-I _{IL}	-	0,4	mA
Input clamping voltage	-I _{IC} = 18,0mA	V _{CC} min.	-V _{ICA}	-	1,5	V
Output voltage	54LS I _{OH} = -400,0µA	V _{CC} min.	V _{OH}	2,5	-	V
	64/74/84LS I _{OH} = -400,0µA		V _{OH}	2,7	-	V
	All types I _{OL} (1) = 4,0mA (1)		V _{OL} (1)	-	0,4	V
	64/74/84LS I _{OL} (2) = 8,0mA (2)		V _{OL} (2)	-	0,5	V

(1) Fan out = 10, (2) Fan out = 20,

*See 3.2.1 of this specification

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Output short circuit current	$V_{IN} = V_{ILA}^*$ or V_{IHB}^* as appropriate† $V_O = 0V$ or $4,5V$ (3)	$V_{CC} \text{ max.}$	$-I_{OS}$	15,0	130,0	mA
Propagation times All types	$T_{amb} = 25^{\circ}C^*$ test conditions as in Sub-group A5	5,0V				
High to Low level	Clock to output		t_{PHL}	-	27,0	ns
Low to High level	Clock to output		t_{PLH}	-	27,0	ns
Maximum clock frequency			$f(\text{clock})$	30,0	-	MHz
Duration of clock pulse			$t_p(\text{clock})$	20,0	-	ns
Set-up time	Data input		$t_{\text{set-up}}$	20,0†	-	ns
	Enable active-level		$t_{\text{set-up}}$	25,0†	-	ns
	Enable inactive-level		$t_{\text{set-up}}$	10,0†	-	ns
Hold time	Data and Enable		t_{hold}	5,0†	-	ns

(3) Only one output at a time, duration $t \leq 1 \text{ sec}$

*See 3.2.1 of this specification

†With reference to the rising edge of the clock pulse

‡Refer to truth table