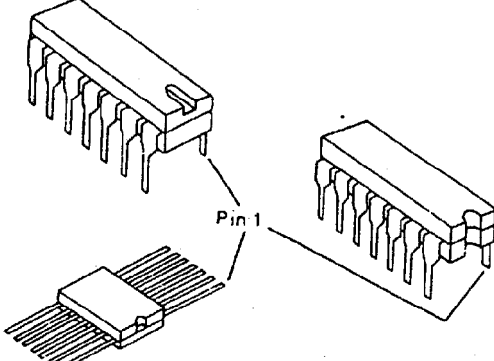


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90103 - 129 ISSUE 1 NOVEMBER 1981  Page 1 of 18 pages
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS393 64LS393 74LS393 84LS393 SEE PD 9002 AND CECC 00 200 For ordering information see clause 1
Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A50B) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	DUAL 4-BIT BINARY COUNTER WITH CLEAR TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200 for details of manufacturers approved to this specification

1.1 Truth table (contd)

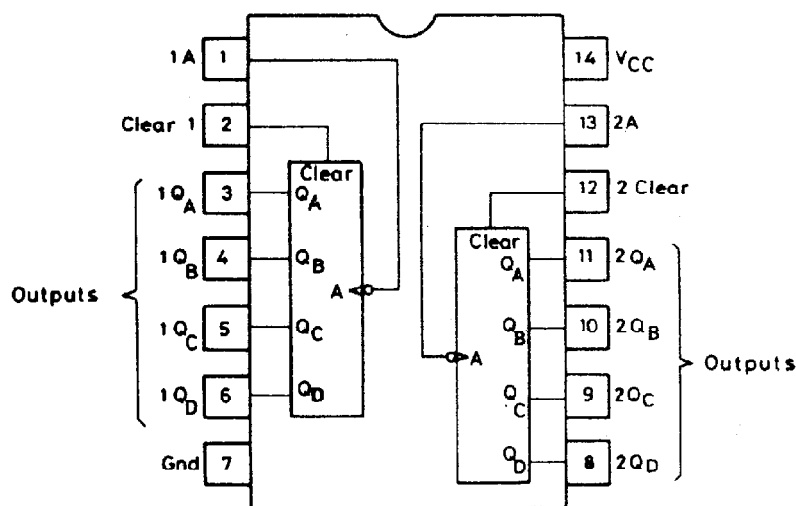
COUNT	CLOCK	OUTPUT			
		Q _D	Q _C	Q _B	Q _A
0	L	L	L	L	L
1	L	L	L	L	H
2	L	L	L	H	L
3	L	L	L	H	H
4	L	L	H	L	L
5	L	L	H	L	H
6	L	L	H	H	L
7	L	L	H	H	H
8	L	H	L	L	L
9	L	H	L	L	H
10	L	H	L	H	L
11	L	H	L	H	H
12	L	H	H	L	L
13	L	H	H	L	H
14	L	H	H	H	L
15	L	H	H	H	H
	H	L	L	L	L

H = High level

L = Low level

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Dual 4-bit binary counter

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS393J	N	W
-25 + 85	84LS393J		
-40 + 85	64LS393J		
-55 +125	54LS393J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

- | | | | |
|-------|--|----------|---|
| 2.1 | Maximum continuous supply voltage | V_{CC} | -0,5V
+7,0V |
| 2.2 | Maximum input voltages | | |
| 2.2.1 | Maximum input voltage | V_I | -0,5V
+7,0V (Clear input)
+5,5V (A input) |
| 2.2.2 | Maximum input voltage between multiple emitter transistor inputs | V_{II} | +5,5V |

- 2.3 Minimum and maximum operating ambient temperatures $T_{amb}(^{\circ}\text{C})$ min. -55 -40 0 -25
max. +125 +85 +70 +85
- 2.4 Minimum and maximum storage temperatures $T_{stg}(^{\circ}\text{C})$ min. -65 (All types)
max. +150

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage Clear input A input	V_{IHA}	All types	7,0 5,5	V V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μA
Maximum applied off level voltage	V_{OZA}	All types	5,5	V
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$) at High level ($V_{OHB} - V_{IHB}$)	V_{NL} V_{NH}	All types 54LS 64/74/84LS	0,3 0,5 0,7	V V V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(\text{V})$	Symbol	Min.	Max.	Unit
Total supply current per package	I_{CC} is measured with all outputs Open, both clear inputs grounded following momentary connection to 4,5V and all other inputs grounded.	$V_{CC} \text{ max.}$	I_{CC}	-	26,0	mA
High level input current	$V_{IH(1)} = 5,5\text{V}$ $V_{IH(1)} = 7,0\text{V}$	$V_{CC} \text{ max.}$	$I_{IH(1)}$	-	0,2	mA
				-	0,1	mA
	$V_{IH(2)} = 2,7\text{V}$	$V_{CC} \text{ max.}$	$I_{IH(2)}$	-	100,0	μA
				-	20,0	μA
Low level input current	$V_{IN} = 0,4\text{V}$	$V_{CC} \text{ max.}$	$-I_{IL}$	-	1,6	mA
				-	0,4	mA
Input clamping voltage	$-I_{IC} = 18,0\text{mA}$	$V_{CC} \text{ min.}$	$-V_{ICA}$	-	1,5	V

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Output voltage		V_{CC} min.				
54LS	$I_{OH} = -400,0\mu A$		V_{OH}	2,5	-	V
64/74/84LS	$I_{OH} = -400,0\mu A$		V_{OH}	2,7	-	V
All types	$I_{OL}(1) = 4,0mA$ (1)		$V_{OL}(1)$	-	0,4	V
64/74/48LS	$I_{OL}(2) = 8,0mA$ (2)		$V_{OL}(2)$	-	0,5	V
Output short circuit current	$V_O = 0V$ (3)	V_{CC} max.	$-I_{OS}$	15,0	130,0	mA
Propagation times	$T_{amb} = 25^{\circ}C^*$ test conditions as in Sub-group A5	5,0V				
All types						
Input A to output Q_A			t_{PHL}	-	20,0	ns
Input A to output Q_D				-	60,0	ns
Clear input to any output				-	39,0	ns
Input A to output Q_A			t_{PLH}	-	20,0	ns
Input A to output Q_D				-	60,0	ns
Maximum Count frequency			$f_{(count)}$	25,0	-	ns
Duration of input pulse			t_p - (input)	20,0	-	ns
Duration of Clear pulse			$t_{p(Clear)}$	20,0	-	ns
Set-up time			t_{set-up}	25,0	-	ns

(1) Fan out = 10, (2) Fan out = 30

(3) Only one output at a time, duration $t \leq 1$ sec

*See clause 3.2.1 of this specification