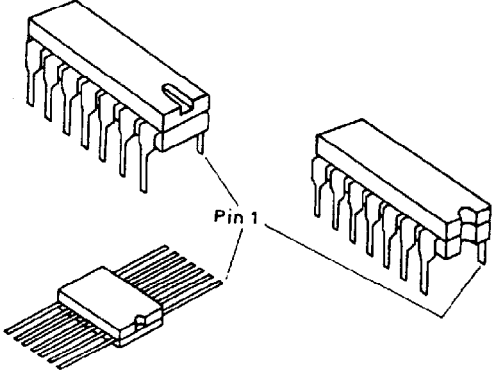


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90103 - 135 ISSUE 1 NOVEMBER 1981  Page 1 of 20 pages
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS95B 64LS95B 74LS95B 84LS95B SEE PD 9002 AND CECC 00 200 For ordering information see clause 1
Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A50B) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	PARALLEL IN/PARALLEL OUT SHIFT RIGHT, SHIFT LEFT 4-BIT SHIFT REGISTER
	TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
 for details of manufacturers approved to this specification

1.1 Truth table (contd)

MODE CONTROL	CLOCKS		INPUTS	PARALLEL				OUTPUTS			
	2 (L)	1 (R)	SERIAL	A	B	C	D	Q _A	Q _B	Q _C	Q _D
H	H	X	X	X	X	X	X	Q _{AO}	Q _{BO}	Q _{CO}	Q _{DO}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q _B †	Q _C †	Q _D †	d	Q _{Bn}	Q _{Cn}	Q _{Dn}	d
L	L	H	X	X	X	X	X	Q _{AO}	Q _{BO}	Q _{CO}	Q _{DO}
L	X	↓	H	X	X	X	X	H	Q _{AO}	Q _{BO}	Q _{CO}
L	X	↓	L	X	X	X	X	L	Q _{AO}	Q _{BO}	Q _{CO}
↑	L	L	X	X	X	X	X	Q _{AO}	Q _{BO}	Q _{CO}	Q _{DO}
↓	L	L	X	X	X	X	X	Q _{AO}	Q _{BO}	Q _{CO}	Q _{DO}
↓	L	H	X	X	X	X	X	Q _{AO}	Q _{BO}	Q _{CO}	Q _{DO}
↑	H	L	X	X	X	X	X	Q _{AO}	Q _{BO}	Q _{CO}	Q _{DO}
↑	H	H	X	X	X	X	X	Q _{AO}	Q _{BO}	Q _{CO}	Q _{DO}

† = Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C, Serial data is entered at input D.

H = High level (steady level)

L = Low level (steady level)

X = Logic level irrelevant (any input including transitions)

a, b, c, d = The level of steady level input at inputs A, B, C, or D respectively.

Q_{AO}, Q_{BO}, Q_{CO}, Q_{DO} = The level of Q_A, Q_B, Q_C or Q_D respectively, before the indicated steady level input conditions were established.

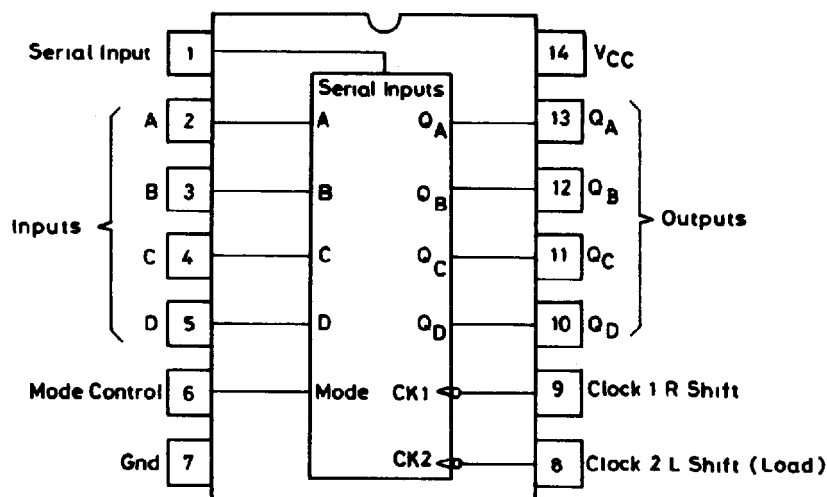
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C or Q_D respectively, before the most recent ↓ transition of the clock.

↑ = Transition of Low to High level

↓ = Transition of High to Low level

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Parallel in/parallel out, shift right,
shift left 4-bit shift register

These 4-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation:

Parallel (Broadside) load
Shift right (the direction of Q_A toward Q_B)
Shift left (the direction of Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input High. The data is loaded into the associated bistable and appears at the output after the High-to-Low transition of the clock 2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the High-to-Low transition of clock 1 when the mode control is Low. Shift left is accomplished on the High-to-Low transition of clock 2, when the mode control is High, by connecting the output of each bistable to the parallel input of the previous bistable (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied simultaneously to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are Low. However, conditions described in the last three lines of the truth table will also ensure that register contents are protected.

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS95BJ	N	W
-25 + 85	84LS95BJ		
-40 + 85	64LS95BJ		
-55 +125	54LS95BJ		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

1.3 Ordering information (contd)

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}						-0,5V +7,0V
2.2	Maximum input voltages							
2.2.1	Maximum input voltage	V_I						-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}						+5,5V
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. max.	-55 +125	-40 +85	0 +70	-25 +85	
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. max.	-65 +150	(All types)			

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μA

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T_{amb} min.	-55	-40	0	-25	°C
T_{amb} max.	+125	+85	+70	+85	
V_{CC} min.	4,5	4,75			V
V_{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	$V_{IL} = 0V$ (1)	$V_{CC} \text{ max.}$	I_{CC}	-	21,0	mA
High level input current	$V_{IN} = 7,0V$	$V_{CC} \text{ max.}$	$I_{IH(1)}$	-	0,2	mA
Clock input			$I_{IH(1)}$	-	0,1	mA
Other inputs	$V_{IN} = 2,7V$		$I_{IH(2)}$	-	40,0	μA
Clock input			$I_{IH(2)}$	-	20,0	μA
Low level input current	$V_{OL} = 0,4V$	$V_{CC} \text{ max.}$	$-I_{IL}$	-	0,8	mA
Clock input			$-I_{IL}$	-	0,4	mA
Other inputs						
Input clamping voltage	$-I_{IC} = 18,0mA$	$V_{CC} \text{ min.}$	$-V_{ICA}$	-	1,5	V
Output voltage	$I_{OH} = -400,0\mu A$	$V_{CC} \text{ min.}$	V_{OH}	2,5	-	V
54LS	$I_{OH} = -400,0\mu A$		V_{OH}	2,7	-	V
64/74/84LS	$I_{OL(1)} = 4,0mA$ (2)		$V_{OL(1)}$	-	0,4	V
All types	$I_{OL(2)} = 8,0mA$ (3)		$V_{OL(2)}$	-	0,5	V
64/74/84LS						
Output short circuit current	$V_O = 0V$ (4) $V_{IL} = 0V$ or 4,5V	$V_{CC} \text{ max.}$	$-I_{OS}$	15,0	130,0	mA

- (1) To all inputs, (2) Fan out = 10, (3) Fan out = 20,
(4) Only one output at a time, duration $t \leq 1 \text{ sec}$

Characteristics	Conditions	V _{CC} (V)	Symbol	Min.	Max.	Unit
Propagation time All types [†]	T _{amb} = 25°C* test conditions as in Sub-group A5	5,0V				
High to Low level from clock			t _{PHL}	-	32,0	ns
Low to High level from clock			t _{PLH}	-	27,0	ns
Maximum clock frequency			f _(clock)	-	25,0	MHz
Minimum duration of clock pulse			t _{p(clock)}	25,0	-	MHz
Set-up time (at Serial A, B, C, D inputs)**			t _{set-up}	20,0	-	ns
Data hold time (at Serial A, B, C, D inputs)**						
54LS			t _{hold}	20,0	-	ns
64/74/84LS			t _{hold}	10,0	-	ns
Time to enable clock 1**			t _{(enable)1}	20,0	-	ns
Time to enable clock 2**			t _{(enable)2}	20,0	-	ns
Time to inhibit clock 1**			t _{(inhibit)1}	20,0	-	ns
Time to inhibit clock 2**			t _{(inhibit)2}	20,0	-	ns

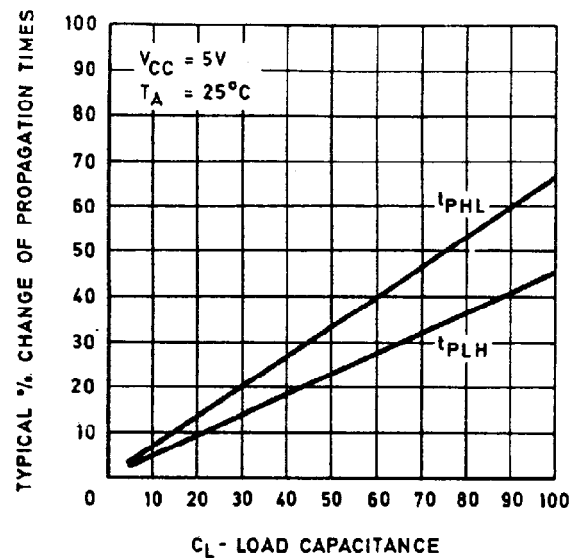
* See 3.2.1 of this specification

**See Appendix A1.3

† Unless marked otherwise

3.3 Supplementary information

3.3.1 Change of typical propagation time with output loading



Propagation time Vs. load capacitance

3.3.2 Variation of propagation time with temperature

