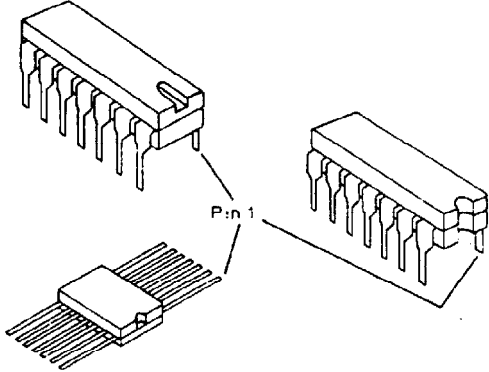


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90103 - 142 ISSUE 1 FEBRUARY 1982 Page 1 of 22 pages
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS197 64LS197 74LS197 84LS197
Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A50B) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	SEE PD 9002 AND CECC 00 200 For ordering information see clause 1 PRESETTABLE BINARY COUNTERS/ LATCHES TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
 for details of manufacturers approved to this specification

1.1 Truth table (contd)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE: Output Q_A connected to Clock 2 input
H = High level
L = Low level

The counters each comprise four master-slave flip-flops which are internally connected to provide a divide-by-two and a divide-by-eight counter. The outputs (Q_A, Q_B, Q_C, Q_D) may be preset by taking the Count/Load input Low and presenting the required data at the Data inputs (A, B, C, D). The outputs change to agree with the Data inputs independent of the level of either Clock input.

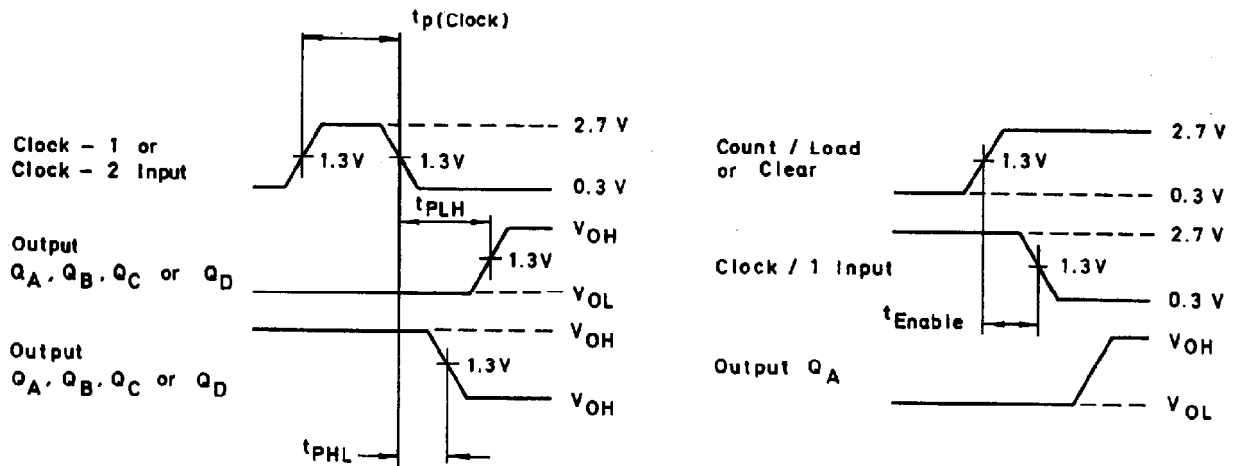
For use as a 4-bit counter, output Q_A may be externally connected to Clock 2 input. Input count pulses are then applied to the Clock 1 input and simultaneous divisions by two, four, eight and sixteen are available at the outputs (see truth table).

For use as a 3-bit counter, the input count pulses are applied to the Clock 2 input and simultaneous divisions by two, four and eight are available at the Q_B, Q_C and Q_D outputs. Independent use of Bistable flip-flop A is available if the Load and Clear functions coincide with those of the three-bit counter.

During counting, information is transferred to the outputs on the negative-going edge of the Clock pulse. Application of a Low to the direct Clear input sets all outputs Low regardless of the levels of the Clocks.

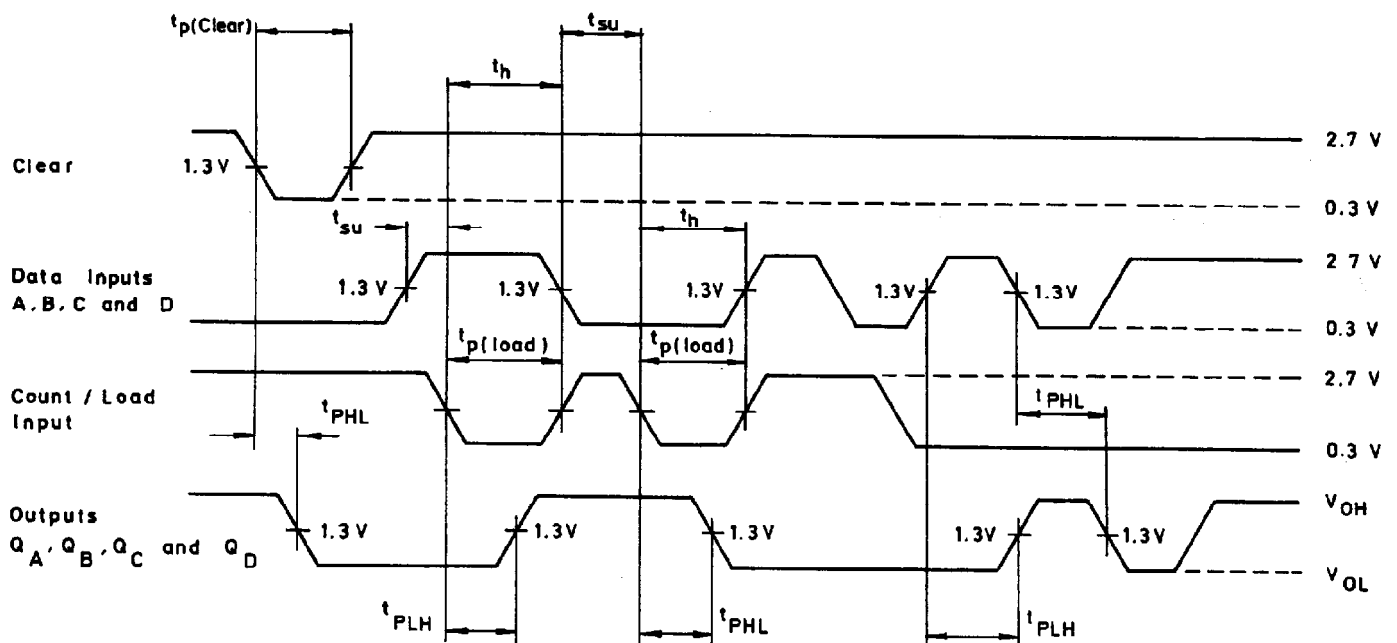
The Counters can be used as 4-bit latches by using the Count/Load input as the strobe and presenting data at the Data inputs. With the Count/Load Low, the outputs directly follow the Data inputs, but with the Count/Load High and the Clock inputs inactive, the outputs remain unchanged.

1.1.1 Typical operating waveform



(a) Clock mode voltage waveform

(b) Clock enable time voltage waveform



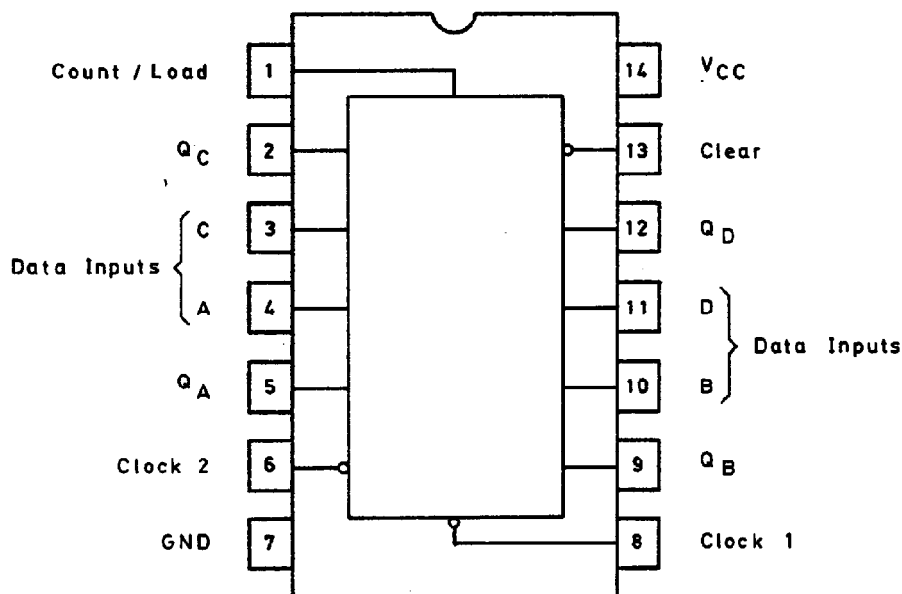
NOTE : t_{su} = Set-up time

t_h = Hold time

(C) = Clear and load voltage waveform

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Presettable binary counters/latches

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS197J	N	W
-25 + 85	84LS197J		
-40 + 85	64LS197J		
-55 +125	54LS197J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}	-0,5V +7,0V				
2.2	Maximum input voltages						
2.2.1	Maximum input voltage	V_I	-0,5V +7,0V				
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}	+5,5V				
				54LS	64LS	74LS	84LS
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. -55 max. +125	-40 +85	0 +70	-25 +85	
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. -65 max. +150	(All types)			

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V

3.1 (contd)

Description	Symbol	Type	Value	Unit
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μA
D.C. noise margin				
at Low level ($V_{ILA} - V_{OLA}$)	V_{NL}	All types	0,3	V
at High level ($V_{OHB} - V_{IHB}$)	V_{NH}	54LS 64/74/84LS	0,5 0,7	V V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	All outputs open circuit. Inputs grounded	V_{CC} max.	I_{CC}	-	27,0	mA
High level input current	$V_{IH(1)} = 5,5V$ Data, Count/Load Clear, Clock 1 and Clock 2	V_{CC} max.	$I_{IH(1)}$	-	0,1	mA
			$I_{IH(1)}$	-	0,2	mA

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
High level input current (contd)	$V_{IH(2)} = 2,7V^*$ Data, Count/Load		$I_{IH(2)}$	-	20,0	μA
	Clear, Clock 1 and Clock 2		$I_{IH(2)}$	-	40,0	μA
Low level input current	$V_{IN} = 0,4V^*$ Data, Count/Load	$V_{CC} \text{ max.}$	$-I_{IL}$	-	0,4	mA
	Clear			-	0,8	mA
	Clock 1			-	2,4	mA
	Clock 2			-	1,3	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	5,0V	$-V_{ICA}$	-	1,5	V
Output voltage	54LS $I_{OH} = -400,0\mu A$	$V_{CC} \text{ min.}$	V_{OH}	2,5	-	V
	64/74/84LS $I_{OH} = -400,0\mu A$		V_{OH}	2,7	-	V
	All types $I_{OL} = 4,0mA$ (1)		V_{OL}	-	0,4	V
	64/74/84LS $I_{OL} = 8,0mA$ (2)		V_{OL}	-	0,5	V
Output short circuit current	$V_{IN} = 0V$ or 4,5V as appropriate $V_O = 0V$ (3)	$V_{CC} \text{ max.}$	$-I_{OS}$	15,0	130,0	mA
Propagation times All types	$T_{amb} = 25^{\circ}C^*$ test conditions as in Sub-group A5	5,0V				
High to Low	Clock 1 to Q_A		t_{PHL}	-	21,0	ns
	Clock 2 to Q_B			-	35,0	ns
	Clock 2 to Q_C			-	63,0	ns
	Clock 2 to Q_D			-	95,0	ns
	A, B, C, D, to Q_A, Q_B, Q_C, Q_D			-	44,0	ns
	Load to Any output			-	45,0	ns
	Carry to Any output			-	51,0	ns

(1) Fan out = 10, (2) Fan out = 20,

(3) Only one output at a time, duration $t \leq 1$ sec

*See 3.2.1 of this specification