

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

BS CECC 90103-168

ISSUE 1

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SPECIFICATION AVAILABLE FROM:- As shown in PD 9002
AND CECC 00 200 ANDTEXAS INSTRUMENTS LIMITED,
MANTON LANE,
BEDFORD, MK41 7PA

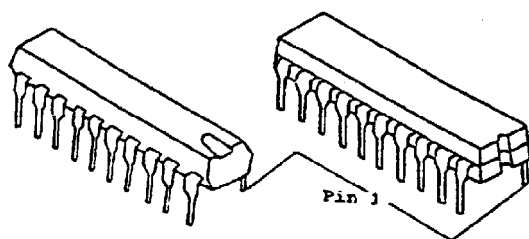
Page 1 of 18 Pages

ELECTRONIC COMPONENTS OF ASSESSED QUALITY

DETAIL SPECIFICATION IN ACCORDANCE WITH:-

BS CECC 90 000 : 1976

BS CECC 90 100 : 1977

Outline not to scale. Isometric projection
Marking information see Clause 1

For detail dimensions — See Appendix 1

MANUFACTURERS TYPE NUMBER

54LS645

64LS645

74LS645

84LS645

SEE PD 9002 AND CECC 00 200
For ordering information
see Clause 1OCTAL BUS TRANSCEIVERS WITH
3-STATE NON-INVERTING OUTPUTSTYPICAL CONSTRUCTION SILICON
MONOLITHIC BIPOLAR LOW POWER
SCHOTTKY TTLASSESSMENT LEVELS R, S, T
AND V1. TYPE DESCRIPTION

1.1. Truth table

Enable $\overline{G}$	Direction Control DIR	Operation
L	L	B data to A bus
L	H	A data to B bus
H	X	isolation

H = High Level

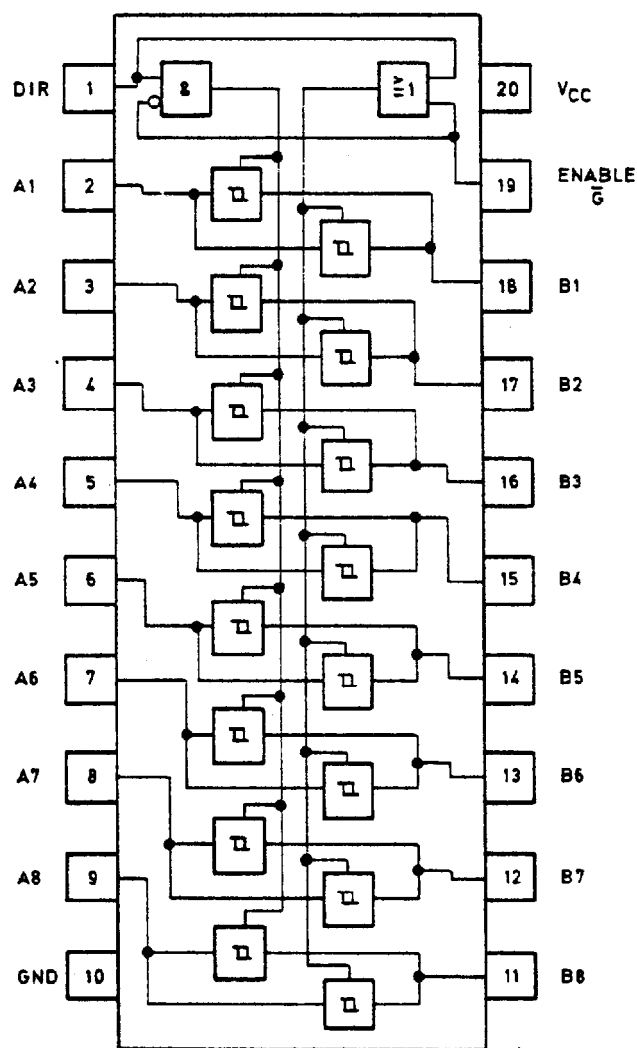
L = Low Level

X = Logic level irrelevant

REFER TO QUALIFIED PRODUCTS LIST PD 9002 AND/OR CECC 00 200
FOR DETAILS OF MANUFACTURERS APPROVED TO THIS SPECIFICATION

1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Octal bus transceiver with 3-level outputs

Three-level device

A device whose output can be driven into a High, Low or high impedance level.

High impedance level

That level of a device in which the output acquires a high impedance characteristic.

High impedance leakage current

The current measured at the output terminal with input conditions applied such as to cause the switching element to be in the high impedance level.

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS645J	N	W
-25 + 85	84LS645J		
-40 + 85	64LS645J		
-55 +125	54LS645J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information.

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}		-0,5V	+7,0V
2.2	Maximum input voltages				
2.2.1	Maximum input voltage	V_I		-0,5V	+7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}		+5,5V	
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min.	-55	-40 0 -25
			max.	+125	+85 +70 +85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min.	-65	(All types)
			max.	+150	

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated

3.1 (Cont'd)

DESCRIPTION	SYMBOL	TYPE	VALUE	UNIT
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4.5 - 5.5 4.75 - 5.25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2.0	V
Maximum value of High level input voltage	V_{IHA}	All types	5.5	V
Minimum value of Low level input voltage	V_{ILB}	-	-0.3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0.5 0.6	V
Maximum value of Low level output current for each output	I_{OL}	54LS 64/74/84LS	12.0 24.0	mA mA
Maximum value of output current for each output at V_{OH}	$-I_{OH}$ $-I_{OH}$	54LS 64/74/84LS	12.0 15.0	mA mA
High impedance level output current	I_{OHZ} $-I_{OLZ}$	All types All types	20.0 400.0	μ A μ A
Maximum applied off-level voltage	V_{OZA}	All types	5.5	V

3.2.1. Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*).

	54LS	64LS	74LS	84LS	
T _{amb} min	-55	-40	0	-25	°C
T _{amb} max	+125	+85	+70	+85	
V _{CC} min.	4.5	4.75			V
V _{CC} max.	5.5	5.25			

3.2.2.

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min	Max	Unit
Total supply current per package	$V_{IL} = 0V$ (1)	V_{CC} max.	I_{CC}			
Outputs High				-	70.0	mA
Outputs Low				-	90.0	mA
Outputs Disabled				-	95.0	mA

(1) To all inputs

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
High level input current		$V_{CC} \text{ max.}$				
DIR and $\bar{G}$ inputs	$V_{IH(1)} = 7,0V$	$V_{CC} \text{ max.}$	$I_{IH(1)}$	-	0,1	mA
A and B inputs	$V_{IN} = 5,5V$			-	0,1	mA
All inputs	$V_{IH(2)} = 2,7V$	$V_{CC} \text{ max.}$	$I_{IH(2)}$	-	20,0	μA
Low level input current	$V_{IL} = 0,4V$	$V_{CC} \text{ max.}$	$-I_{IL}$	-	0,4	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	$V_{CC} \text{ min.}$	$-V_{ICA}$	-	1,5	V
Output voltage		$V_{CC} \text{ min.}$				
54LS	$-I_{OH} = 12,0mA$		V_{OH}	2,0	-	V
64/74/84LS	$-I_{OH} = 15,0mA$		V_{OH}	2,0	-	V
All types	$I_{OL(1)} = 12,0mA$ (2)		$V_{OL(1)}$	-	0,4	V
64/74/84LS	$I_{OL(2)} = 24,0mA$ (3)		$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_O = 0V \text{ or } 4,5V^{(4)}$	$V_{CC} \text{ max.}$	$-I_{OS}$	40,0	225,0	mA
Propagation time		5,0V				
All types	$T_{amb} = 25^{\circ}C^*$		t_{PLH}	-	15,0	ns
	test conditions		t_{PHL}	-	15,0	ns
	as in Sub-group A5		t_{PLZ}	-	40,0	ns
	$C_L = 45pF$		t_{PHZ}	-	40,0	ns
			t_{PLZ}	-	25,0	ns
	$C_L = 5pF$		t_{PHZ}	-	25,0	ns

(2) Fan out = 30, (3) Fan out = 60,

(4) Only one output at a time, duration $t \leq 1 \text{ sec}$

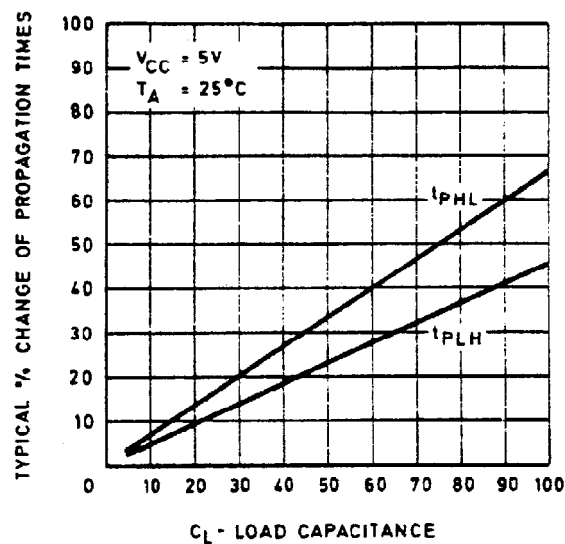
* See 3.2.1 of this specification

3.3 Supplementary information

3.3.1 D.C. noise margin

Low level $V_{ILA} - V_{OLA} = V_{NL}$ High level $V_{OHB} - V_{IHB} = V_{NL}$

3.3.2 Change of typical propagation time with output loading



Propagation times Vs. load capacitance

3.3.3 Variation of propagation time with temperature

