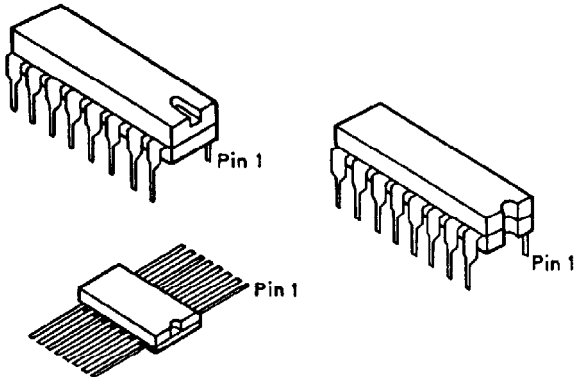


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	BS CECC 90103 - 172 ISSUE 1 DECEMBER 1981 Page 1 of 22 pages 
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS395A 64LS395A 74LS395A 84LS395A
Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A50C) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	SEE PD 9002 AND CECC 00 200 For ordering information see clause 1 4-BIT CASCADABLE SHIFT REGISTER WITH THREE LEVEL OUTPUTS TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.1 Truth table (contd)

INPUTS								TRI-LEVEL OUTPUTS				CASCADE OUTPUT Q_D'
CLEAR	LOAD/SHIFT CONTROL	CLOCK	SERIAL	PARALLEL				Q_A	Q_B	Q_C	Q_D	
				A	B	C	D					
L	X	X	X	X	X	X	X	L	L	L	L	L
H	H	H	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}	Q_{DO}
H	H	↓	X	a	b	c	d	a	b	c	d	d
H	L	H	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}	Q_{DO}
H	L	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
H	L	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}

H = High level

L = Low level

X = Logic level irrelevant - (any input including transition)

↓ = Transition from High to Low level

 Q_{AO} , Q_{BO} , Q_{CO} , Q_{DO} = The level of Q_A , Q_B , Q_C or Q_D respectively, before the indicated steady level input conditions were established.

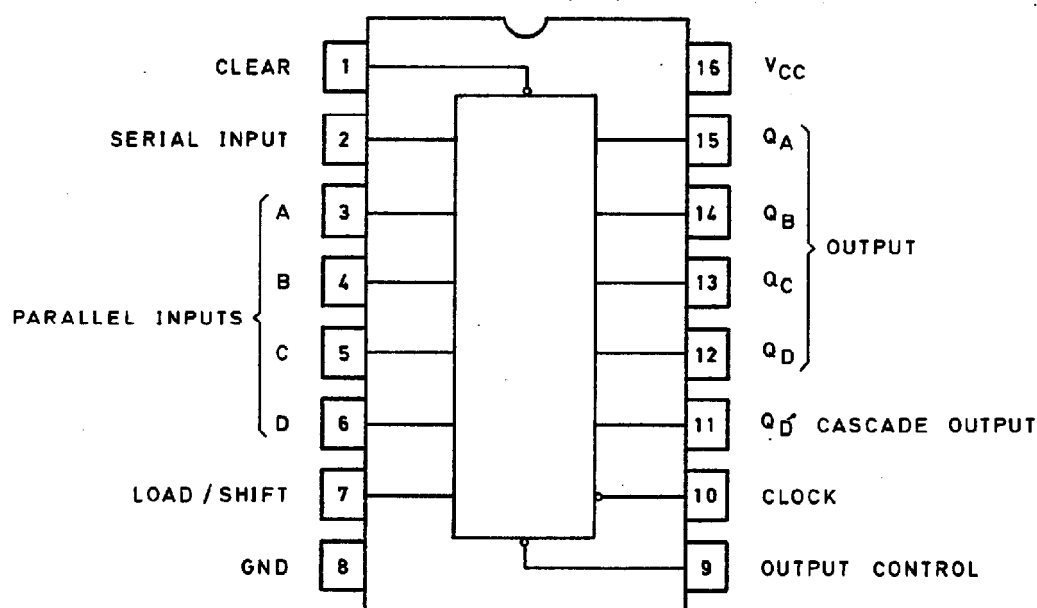
 Q_{An} , Q_{Bn} , Q_{Cn} , Q_{Dn} = The level of Q_A , Q_B , Q_C or Q_D respectively, before the more recent transition of the clock

a, b, c, d = The level of steady level input at inputs A, B, C or D respectively

When the output control is High, the three level outputs are disabled to the high impedance level however, sequential operation of the registers and the output Q_D' are not affected.

1.2 Terminal identification, type designation and marking.

1.2.1 Terminal identification



4-bit cascadable shift register with three level outputs

1.2.1 Terminal identification (contd)

Three level device

A device whose output can be driven into a High, Low or high impedance level.

High impedance level

That level of a device in which the output acquires a high impedance characteristic.

High impedance leakage current

The current measured at the output terminal with input conditions applied such as to cause the switching element to be in the high impedance level.

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS395AJ	N	W
-25 + 85	84LS395AJ		
-40 + 85	64LS395AJ		
-55 +125	54LS395AJ		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1).

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}	-0,5V +7,0V
2.2	Maximum input voltages		
2.2.1	Maximum input voltage	V_I	-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}	+5,5V

			54LS	64LS	74LS	84LS
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. -55 max. +125	-40 +85	0 +70	-25 +85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. -65 max. +150	(All types)		

3. Recommended operating conditions and associated characteristics (not for inspection purposes).

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output (Q_A, Q_B, Q_C, Q_D)	I_{OLA}	54LS 64/74/84LS 54LS 64/74/84LS	12,0 24,0 4,0 8,0	mA mA mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	54LS 64/74/84LS	-1,0 -2,6	mA mA
Maximum value of High level output current for Cascade output Q_D	I_{OHA}	All types	-400,0	μA

3.1 (contd)

Description	Symbol	Type	Value	Unit
High impedance level output (leakage) current $V_O = 2,7V$ $V_O = 0,4V$	I_{OHZ}	All types	20,0	μA
	$-I_{OLZ}$	All types	20,0	μA
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$) at High level ($V_{OHB} - V_{IHB}$)	V_{NL}	All types	0,3	V
	V_{NH}	54LS	0,5	V
		64/74/84LS	0,7	V
Minimum value of off-level output voltage	V_{OZA}	All types	5,5	V

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	Output control at 4,5V and a momentary 3,0V, then ground, applied to clock input.	V_{CC} max.	$I_{CC(1)}$	-	34,0	mA
	Output control and clock input grounded.	V_{CC} max.	$I_{CC(2)}$	-	31,0	mA

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
High level input current	$V_{IH(1)} = 7,0V$ $V_{IH(2)} = 2,7V$	$V_{CC} \text{ max.}$ $V_{CC} \text{ max.}$	$I_{IH(1)}$ $I_{IH(2)}$	-	0,1 20,0	mA μA
Low level input current	$V_{IN} = 0,4V$ to each input in turn, other inputs at 7,0V	$V_{CC} \text{ max.}$	$-I_{IL}$	-	0,4	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	$V_{CC} \text{ min.}$	$-V_{ICA}$	-	1,5	V
Output voltage		$V_{CC} \text{ min.}$				
Q_A, Q_B, Q_C, Q_D 54LS	$I_{OH} = -I_{OHA}^*$ $I_{OH} = -I_{OHA}^*$		V_{OH} V_{OH}	2,4 2,5	-	V V
64/74/84LS Q_D Q_A, Q_B, Q_C, Q_D All types	$I_{OH} = -I_{OHA}^*$ $I_{OL(1)} = 12,0mA \text{ (1)}$		V_{OH} $V_{OL(1)}$	2,7 -	- 0,4	V V
Q_A, Q_B, Q_C, Q_D 64/74/84LS	$I_{OL(2)} = 24,0mA \text{ (2)}$		$V_{OL(2)}$	-	0,5	V
All types Q_D	$I_{OL(3)} = 4,0mA \text{ (3)}$		$V_{OL(3)}$	-	0,4	V
64/74/84LS Q_D	$I_{OL(4)} = 8,0mA \text{ (4)}$		$V_{OL(4)}$	-	0,5	V
Output short circuit current	$V_{IN} = 0V$ or 4,5V to inputs in accordance with truth table to give High level condition each output $V_O = 0V$ or 4,5V (5)	$V_{CC} \text{ max.}$	$-I_{OS}$	15,0	130,0	mA
Propagation times						
All types	$T_{amb} = 25^\circ C^*$ test conditions as in Sub-group A5	5,0V				
Low to High level to all outputs			t_{PLH}	-	30,0	ns
High to Low level outputs			t_{PHL}	-	35,0	ns
Q_A, Q_B, Q_C, Q_D To output Q_D				-	30,0	ns

(1) Fan out = 30, (2) Fan out = 60, (3) Fan out = 10,

(4) Fan out = 20 (5) Only one output at a time, duration $t \leq 1 \text{ sec}$

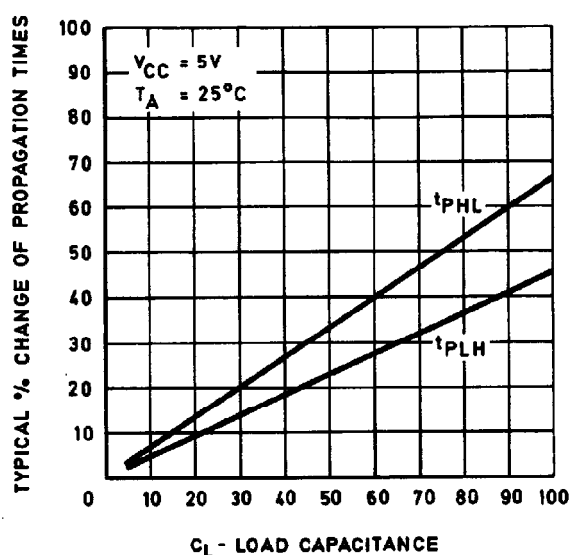
*See 3.2.1 of this specification

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Output enable to High level			t_{PZH}	-	32,0	ns
Output enable to Low level			t_{PZL}	-	30,0	ns
Output disable from High level	$C_L = 5,0pF$		t_{PHZ}	-	17,0	ns
Output disable from Low level	$C_L = 5,0pF$		t_{PLZ}	-	20,0	ns
Maximum clock frequency			f_{clock}	25,0	-	MHz
Duration of clock pulse			$t_{p(clock)}$	25,0	-	ns
Set-up time Data input Load/Shift input			t_{set-up}	25,0	-	ns
			t_{set-up}	40,0	-	ns
Data hold time			t_{hold}	20,0	-	ns

3.3 Supplementary information

3.3.1 Change of typical propagation time with output loading



Propagation time Vs. load capacitance