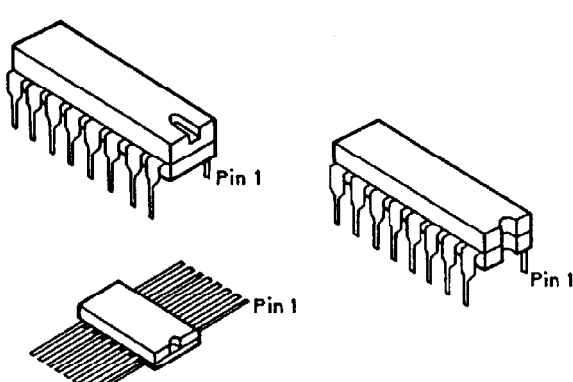


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	BS CECC 90103 - 173 ISSUE 1 NOVEMBER 1981 Page 1 of 20 pages
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 54LS669 64LS669 74LS669 84LS669
Outline not to scale: Isometric projection Marking information see clause 1  Refer to IEC 191-1-50a (type A50C) Dual-in-Line (plastic or ceramic) refer to Appendix A1.3 Flatpack (metal or ceramic)	SEE PD 9002 AND CECC 00 200 For ordering information see clause 1 SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTER TYPICAL CONSTRUCTION SILICON MONOLITHIC BIPOLAR TTL-LOW-POWER SCHOTTKY ASSESSMENT LEVELS R, S, T AND V

1. Type description

1.1 Truth table (see page 2)

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.1 Truth table

Operating mode	INPUTS						OUTPUTS	
	Clock	$U/\bar{D}$	Enable $\bar{P}$	Enable $\bar{T}$	Load	$D_{(n)}$	$Q_{(n)}$	Ripple carry
Parallel load	↑	X	X	X	L	L	L	(a)
	↑	X	X	X	L	H	H	(a)
Count up	↑	H	L	L	H	X	Count up	(a)
Count down	↑	L	L	L	H	X	Count down	(a)
Hold	↑	X	H	X	H	X	Q_n	(a)
	↑	X	X	H	H	X	Q_n	H

H = High level
 L = Low level
 X = Logic level irrelevant
 ↑ = Low to High level clock transition
 Q_n = Level of Q before the most recent active transition indicated by ↑

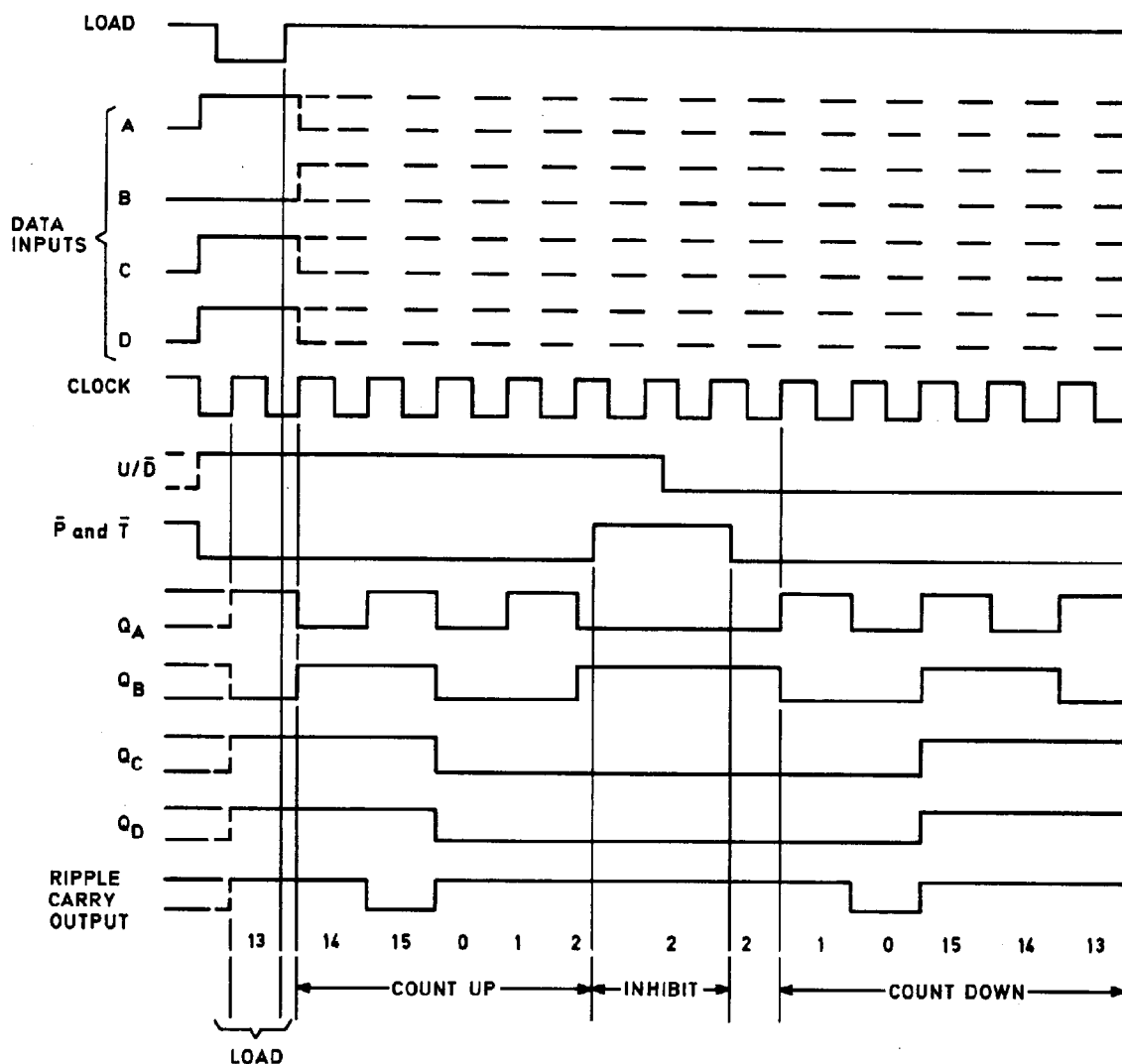
NOTE: (a) = The ripple carry output is Low when enable T is Low and the counter is at terminal count.
 Terminal count up is (H H H H) and terminal count down is (L L L L).

1.1.1 Typical operating waveform diagram

Following sequence given below:

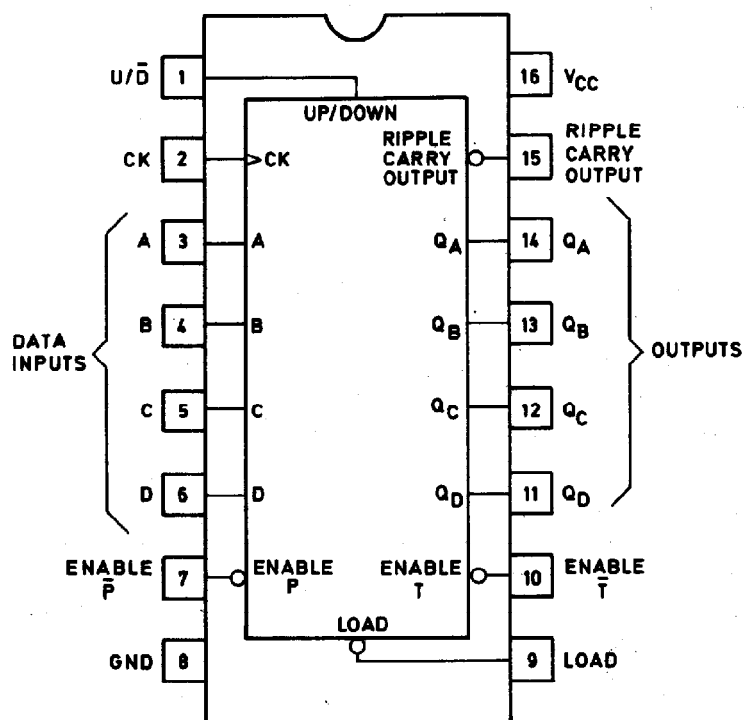
- (1) Load to binary thirteen
- (2) Count up to fourteen, fifteen (max.), zero, one and two
- (3) Inhibit
- (4) Count down to one, zero (min.), fifteen, fourteen and thirteen

1.1.1 (contd)



1.2 Terminal identification, type designation and marking

1.2.1 Terminal identification



Synchronous 4-bit Up/Down binary counter

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS669J	N	W
-25 + 85	84LS669J		
-40 + 85	64LS669J		
-55 +125	54LS669J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information.

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1).

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}						-0,5V +7,0V
2.2	Maximum input voltages							
2.2.1	Maximum input voltage	V_I						-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}						+5,5V
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min.	54LS -55	64LS -40	74LS 0	84LS -25	
			max.	+125	+85	+70	+85	
2.4	Minimum and maximum storage temperatures	$T_{amb}(^{\circ}C)$	min.	-65	(All types)			
			max.	+150				

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V

3.1 (contd)

Description	Symbol	Type	Value	Unit
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	$-I_{OHA}$	All types	400,0	μA

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	$V_{IL} = 0V$ (1)	V_{CC} max.	I_{CC}	-	34,0	mA
High level input current A,B,C,D, $\bar{P}$ and $U/\bar{D}$ Clock and $\bar{T}$ Load A,B,C,D, $\bar{P}$ and $U/\bar{D}$ Clock and $\bar{T}$ Load	$V_{IH(1)} = 7,0V$	V_{CC} max.	$I_{IH(1)}$	-	0,1	mA
				-	0,1	mA
				-	0,2	mA
	$V_{IH(2)} = 2,7V$	V_{CC} max.	$I_{IH(2)}$	-	20,0	μA
				-	20,0	μA
				-	40,0	μA
Low level input current A,B,C,D, $\bar{P}$ and $U/\bar{D}$ Clock and $\bar{T}$ Load	$V_{IL} = 0,4V$	V_{CC} max.	$-I_{IL}$	-	0,4	mA
				-	0,4	mA
				-	0,8	mA
Input clamping voltage	$-I_{IC} = 18,0mA$	V_{CC} min.	$-V_{ICA}$	-	1,5	V

(1) To all inputs

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Output voltage						
54LS	$-I_{OH} = 400,0\mu A$	$V_{CC} \text{ min.}$	V_{OH}	2,5	-	V
64/74/84LS	$-I_{OH} = 400,0\mu A$		V_{OH}	2,7	-	V
All types	$I_{OL(1)} = 4,0mA \text{ (2)}$		V_{OL}	-	0,4	V
64/74/84LS	$I_{OL(2)} = 8,0mA \text{ (3)}$		V_{OL}	-	0,5	V
Output short circuit current	$V_O = 0V \text{ or } 4,5V \text{ (4)}$	$V_{CC} \text{ max.}$	$-I_{OS}$	20,0	100,0	mA
Propagation times						
All types	$T_{amb} = 25^\circ C^*$ test conditions as in Sub-group A5	5,0V				
From Clock to Ripple Carry			t_{PLH}	-	40,0	ns
From Enable $\bar{T}$ to Ripple Carry				-	17,0	ns
From Clock to Any Q				-	27,0	ns
From Up/Down to Ripple Carry	See Note (5)			-	35,0	ns
From Clock to Ripple Carry			t_{PHL}	-	60,0	ns
From Enable $\bar{T}$ to Ripple Carry				-	45,0	ns
From Clock to Any Q				-	27,0	ns
From Up/Down to Ripple Carry	See Note (5)			-	40,0	ns
Maximum clock frequency			f_{clock} t_{pclock}	-	25,0	MHz ns
Set-up time						
Data inputs A,B,C,D			t_{su}	20,0	-	ns
Enable $\bar{P}$ or $\bar{T}$				35,0	-	ns
Load				25,0	-	ns
Up/Down				30,0	-	ns
Hold time			t_{hold}	0	-	ns

(2) Fan out = 10, (3) Fan out = 20, (4) Only one output at a time, duration $t \leq 1 \text{ sec.}$

(5) The propagation delay time must be measured with the counter at either a maximum or minimum count. As the logic level of the Up/Down input is changed, the Ripple Carry output will follow.

If the count is minimum (0) the Ripple Carry transition will be in phase.

If the count is maximum (15) the Ripple Carry output transition will be out of phase.

* See 3.2.1 of this specification