

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 AND

BS CECC 90103 - 174

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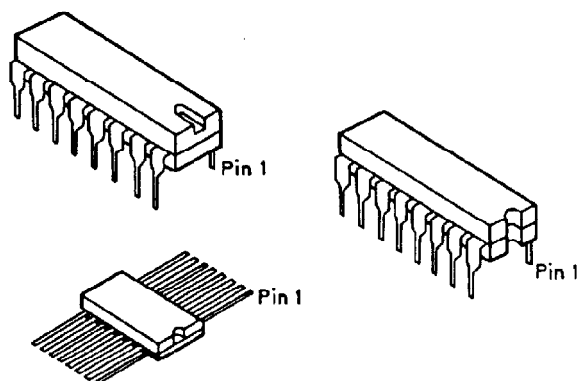
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH:

BS CECC 90 000 : 1976
BS CECC 90 100 : 1977

MANUFACTURERS TYPE NUMBER

54LS670
64LS670
74LS670
84LS670

Outline not to scale: Isometric projection
Marking information see clause 1



Refer to IEC 191-1-50a (type A50C)
Dual-in-Line (plastic or ceramic)
refer to Appendix A1.3
Flatpack (metal or ceramic)

SEE PD 9002 AND CECC 00 200
For ordering information see
clause 1

4-BY-4 REGISTER FILES WITH THREE LEVEL OUTPUTS

TYPICAL CONSTRUCTION
SILICON MONOLITHIC
BIPOLAR TTL-LOW-POWER
SCHOTTKY

ASSESSMENT LEVELS
R, S, T AND V

1. Type description

1.1 Truth table

WRITE TABLE

WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	$Q=D$	Q_0	Q_0	Q_0
L	H	L	Q_0	$Q=D$	Q_0	Q_0
H	L	L	Q_0	Q_0	$Q=D$	Q_0
H	H	L	Q_0	Q_0	Q_0	$Q=D$
X	X	H	Q_0	Q_0	Q_0	Q_0

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.1 Truth table (contd)

READ TABLE

READ INPUTS			OUTPUTS			
R _B	R _A	G _R	Q1	Q2	Q3	Q4
L	L	L	WOB1	WOB2	WOB3	WOB4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

H = High level

L = Low level

X = Logic level irrelevant

Z = High-impedance level (output disabled)

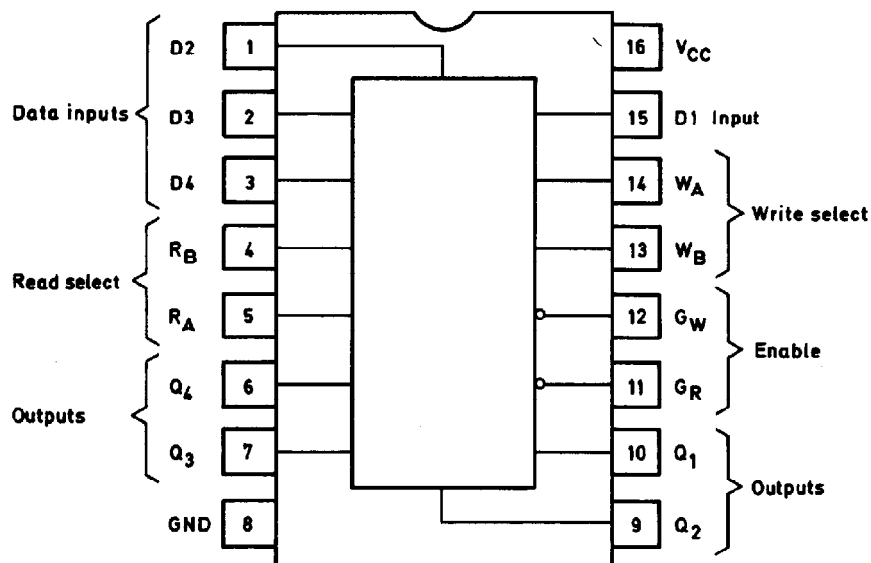
(Q=D) = The four selected internal bistable outputs will assume the level applied to the four external data inputs.

Q₀ = The level of Q before the indicated input conditions were established.

1-W3B4 = The first bit of word 0 through the fourth bit of word 3.

1.2 Terminal identification, type designation and marking.

1.2.1 Terminal identification



4-by-4 register files with three level outputs

Definitions

Three level device:

A device whose output can be driven into the High, Low or high-impedance level.

High-impedance level:

That level of a device in which the output acquires a high-impedance level.

High-impedance (leakage) output current:

The current measured at the output terminal with input conditions applied such as to cause the switching element to be in the high-impedance level.

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS670J	N	W
-25 + 85	84LS670J		
-40 + 85	64LS670J		
-55 +125	54LS670J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1).

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}	-0,5V +7,0V
2.2	Maximum input voltages		
2.2.1	Maximum input voltage	V_I	-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}	+5,5V

2. Limiting conditions of use (contd)

			54LS	64LS	74LS	84LS
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. -55 max. +125	-40 +85	0 +70	-25 +85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. -65 max. +150	(All types)		

3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	$-I_{OHA}$	54LS 64/74/84LS	1,0 2,6	mA mA
High-impedance level output current	I_{OHZ} $-I_{OLZ}$	All types	20,0 20,0	μA μA

3.2 Associated characteristics

3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

3.2.1 (contd)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(\text{V})$	Symbol	Min.	Max.	Unit
Total supply current per package Outputs open circuit, address inputs at zero volts, Data and enable inputs at 4,5V	$V_{IL} = 0\text{V}$ (1)	V_{CC} max.	I_{CC}	-	50,0	mA
High level input current (Any D, R or W) GW GR (Any D, R or W) GW GR	$V_{IH(1)} = 7,0\text{V}$	V_{CC} max.	$I_{IH(1)}$	-	0,1	mA
				-	0,2	mA
				-	0,3	mA
	$V_{IH(2)} = 2,7\text{V}$	V_{CC} max.	$I_{IH(2)}$	-	20,0	μA
				-	40,0	μA
				-	60,0	μA
Low level input current (Any D, R or W) GW GR	$V_{IN} = V_{OLA}$	V_{CC} max.	$-I_{IL}$	-	0,4	mA
				-	0,8	mA
				-	1,2	mA
Input clamping voltage	$-I_{IC} = 18,0\text{mA}$	V_{CC} min.	$-V_{ICA}$	-	1,5	V
Output voltage 54LS 64/74/84LS All types 64/74/84LS	$-I_{OH} = 1,0\text{mA}$	V_{CC} min.	V_{OH}	2,4	-	V
	$-I_{OH} = 2,6\text{mA}$	V_{CC} min.	V_{OH}	2,4	-	V
	$I_{OL(1)} = 4,0\text{mA}$ (2)	V_{CC} min.	$V_{OL(1)}$	-	0,4	V
	$I_{OL(2)} = 8,0\text{mA}$ (3)	V_{CC} min.	$V_{OL(2)}$	-	0,5	V

(1) To all inputs, (2) Fan out = 10 (3) Fan out = 20

3.2.2 (contd)

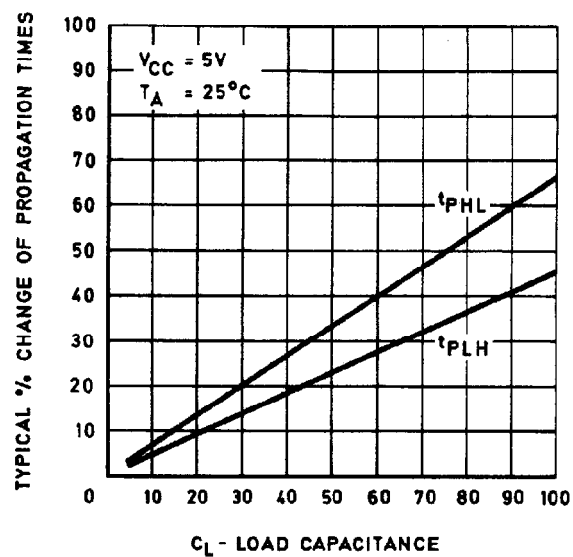
Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Output short circuit current	$V_O = 0V$ (4) $V_{IL} = 0V$	$V_{CC} \text{ max.}$	$-I_{OS}$	15,0	130,0	mA
Propagation time All types Read select to Any Q Write enable to Any Q Data to Any Q Read select to Any Q Write select to Any Q Data to Any Q	$T_{amb} = 25^\circ C^*$ test conditions as in Sub-group A5 $C_L = 15pF$	5,0V	t_{PLH} t_{PHL}	- - - - - - -	40,0 45,0 45,0 45,0 50,0 40,0	ns ns ns ns ns ns ns
Output enable to High level			t_{PZH}	-	35,0	ns
Output enable to Low level			t_{PZL}	-	40,0	ns
Output disable from High level	$(C_L = 5pF)$		t_{PHZ}	-	50,0	ns
Output disable from Low level	$(C_L = 5pF)$		t_{PLZ}	-	35,0	ns
Minimum duration of read write enable pulse		5,0V	$t_{p(GW/R)}$	25,0	-	ns
Minimum set-up time: Write select with respect to Write enable Data input with respect to Write enable			t_{set-up}	15,0 10,0	- -	ns ns
Minimum hold time: Write select with respect to Write enable Data input with respect to Write enable			t_{hold}	5,0 15,0	- -	ns ns
Minimum latch time (new data to latch output)			t_{latch}	25,0	-	ns

(4) Only one output at a time, duration $t \leq 1 \text{ sec}$

*See 3.2.1 of this specification

3.3 Supplementary information

3.3.1 Change of typical propagation time with output loading



Propagation time Vs. load capacitance

3.3.2 Variation of propagation time with temperature

