

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

SPECIFICATION AVAILABLE FROM:- As shown in PD 9002
AND CECC 00 200 AND

TEXAS INSTRUMENTS LIMITED,
MANTON LANE,
BEDFORD, MK41 7PA

BS CECC 90103-179

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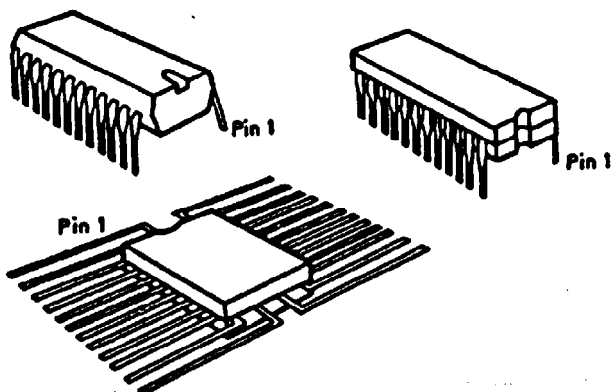
ELECTRONIC COMPONENTS OF ASSESSED QUALITY

DETAIL SPECIFICATION IN ACCORDANCE WITH:-

BS CECC 90 000 : 1982

BS CECC 90 100 : 1977

Outline not to scale. Isometric projection
Marking information see Clause 1



IEC 191-2 (Type A51 D)
Dual-in-line (plastic or ceramic)
Appendix A1.3 Flatpack (metal or ceramic)

MANUFACTURERS TYPE NUMBER

54LS673

64LS673

74LS673

84LS673

SEE PD 9002 AND CECC 00 200
For ordering information
see Clause 1

16 BIT SHIFT REGISTERS

TYPICAL CONSTRUCTION
SILICON MONOLITHIC
BIPOLAR TTL LOW POWER SCHOTTKY

ASSESSMENT LEVELS R, S, T
AND V

1. TYPE DESCRIPTION

1.1. Truth table (see Page 2)

REFER TO QUALIFIED PRODUCTS LIST PD 9002 AND/OR CECC 00 200
FOR DETAILS OF MANUFACTURERS APPROVED TO THIS SPECIFICATION

1.1. Truth Table (Cont'd)

INPUTS					SER/ Q15	SHIFT REGISTER FUNCTIONS				STORAGE REGISTER FUNCTIONS	
$\overline{CS}$	R/W	EN CLK	STECN	MODE/ STACLE		SHIFT	READ FROM SERIAL OUTPUT	WRITE INTO SERIAL INPUT	PARALLEL LOAD	CLEAR	LOAD
H	X	X	X	X	Z	NO	NO	NO	NO		NO
H	X	X	L	X						YES	
L	L	1	X	X	Z	YES	NO	YES	NO		NO
L	H	X	X	X	Q15		YES	NO			NO
L	H	X	X	L	Q14n	YES	YES	NO	NO		NO
L	H	1	L	H	L	NO	YES		YES	YES	NO
L	H	1	H	H	V15n	NO	YES		YES	NO	NO
L	L	X	H	1	Z		NO		NO	NO	YES

The 75873 is a 16-bit shift register and a 16-bit storage register in a single 24-pin package. A three-state input/output (SER/Q15) port to the shift register allows serial entry and/or reading of data. The storage register is connected in a parallel data loop with the shift register and may be asynchronously cleared by taking the store-clear input low. The storage register may be parallel loaded with shift-register data to provide shift-register status via the parallel outputs. The shift register can be parallel loaded with the storage-register data upon command.

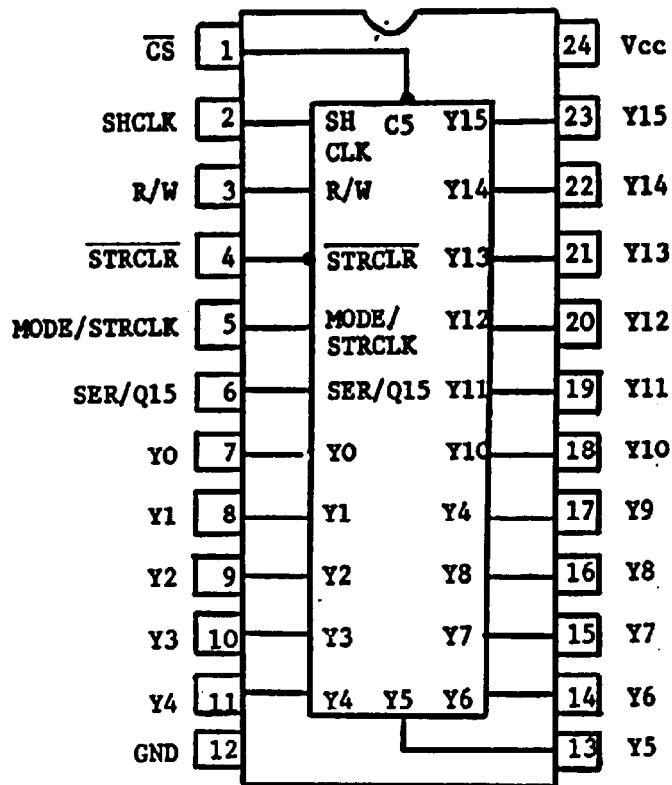
A high logic level at the chip-select ($\overline{CS}$) input disables both the shift-register clock and the storage-register clock and places SER/Q15 in the high-impedance state. The store-clear function is not disabled by the chip select.

Caution must be exercised to prevent false clocking of either the shift register or the storage register via the chip-select input. The shift clock should be low during the low-to-high transition of chip select and the store clock should be low during the high-to-low transition of chip select.

H = high level (steady state)
L = low level (steady state)
1 = transition from low to high level
1 = transition from high to low level
X = irrelevant (any input including transitional)
Z = high impedance, input mode
Q14n = contents of 14th bit of the shift register before the most recent 1 transition of the clock.
Q15 = present contents of 15th bit of the shift register
V15n = contents of the 15th bit of the storage register before the most recent 1 transition of the clock.

1.2. Termination Identification, Type Designation and Marking

1.2.1. Terminal Identification



1.2.2. Type Designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS673J	N	W
-25 + 85	84LS673J		
-40 + 85	64LS673J		
-55 +125	54LS673J		

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1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1).

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}	-0,5V +7,0V
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2.2	Maximum input voltages	
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2.2.1	Maximum input voltage	SER/Q15	V_I	-0,5V +5,5V
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ALL OTHERS

2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}	-0,5V +5,5V +5,5V
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54LS 64LS 74LS 84LS

2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min. -55 max. +125	-40 +85	0 +70	-25 +85
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2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min. -65 max. +150	(All types)
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3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

3.1. (Cont'd)

DESCRIPTION	SYMBOL	TYPE	VALUE	UNIT
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4.5 - 5.5 4.75- 5.25	V V
Minimum value of high level input voltage	V_{IHB}	All types	2.0	V
Maximum value of high level input voltage	V_{IHA}	All types	5.5	V
Minimum value of low level input voltage	V_{ILB}	All types	-0.3	V
Maximum value of low level input voltage	V_{ILA}	54LS 64/74/84LS	0.7 0.8	V
Maximum value of low level output current for each output Y ₀ thru Y ₁₅ SER/Q15	I_{OLA} I_{OLA}	54LS 64/74/84LS 54LS 64/74/84LS	4.0 8.0 -1.0 -2.6	mA mA mA mA
Maximum value of output current for each output of V_{OH} Y ₀ thru Y ₁₅ SER/Q15	$-I_{OHA}$ $-I_{OHA}$	All types 54LS 64/74/84LS	400.0 12.0 24.0	μ A mA mA

3.2 Associated Characteristics

- 3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*).

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

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3.2.2

CHARACTERISTICS	CONDITIONS	$V_{CC}(V)$	SYMBOL	MIN.	MAX.	UNIT
Total supply current per package	$V_{IL} = 0V$ (1) $V_{IH} = 4.5V$	$V_{CC} \text{ max.}$	I_{CC}	-	80.0	mA
High level input current	SER/Q15 $V_1 = 5.5V$ OTHERS $V_1 = 7.0V$ SER/Q15 $V_1 = 2.7V$ OTHERS $V_1 = 2.7V$	$V_{CC} \text{ max.}$	$I_{IH(1)}$	-	0.1	mA
			$I_{IH(2)}$	-	4.0	μA
			$I_{IH(2)}$	-	2.0	μA
Low level input current	$V_{IL} = 0.4V$	$V_{CC} \text{ max.}$	$-I_{IL}$	-	0.4	mA
Input clamping voltage	$-I_{IC} = 18.0mA$	$V_{CC} \text{ min.}$	$-V_{ICA}$	-	1.5	V
Output voltage SER/Q15 54LS SER/Q15 64/74/84LS YO thru Y15 54LS YO thru Y15 64/74/84LS SER/Q15 All Types SER/Q15 64/74/84LS YO thru Y15 All Types YO thru Y15 64/74/84LS	$I_{OH} = \text{max.}$	$V_{CC} \text{ min.}$	V_{OH}	2.4	-	V
			V_{OH}	2.4	-	V
			V_{OH}	2.5	-	V
			V_{OH}	2.7	-	V
	$I_{OL(1)} = 12mA$ (2) $I_{OL(2)} = 24mA$ (3) $I_{OL(1)} = 4mA$ (2) $I_{OL(2)} = 8mA$ (3)	$V_{CC} \text{ min.}$	$V_{OL(1)}$	-	0.4	V
			$V_{OL(2)}$	-	0.5	V
			$V_{OL(1)}$	-	0.4	V
			$V_{OL(2)}$	-	0.5	V
Output short circuit current SER/Q15 YO thru Y15	$V_O = 0V$ (4) $V_{IL} = 0V$	$V_{CC} \text{ max.}$	$-I_{OS}$	30.0	130.0	mA
			$-I_{OS}$	20.0	100.0	mA
Propagation times All Types	$T_{amb} = 25^\circ C$ test conditions as in Subgroup A5	5.0V				
Frequency of operation						
SH CLK $\rightarrow$ SER/Q15			f_{max}	20.0	-	MHz
STRCLR $\rightarrow$ YO thru Y15			t_{PHL}	-	40.0	ns
MODE/STRCLK $\rightarrow$			t_{PLH}	-	45.0	ns
YO thru Y15			t_{PHL}	-	45.0	ns
SH CLK $\rightarrow$ SER/Q15			t_{PLH}	-	33.0	ns
			t_{PHL}	-	40.0	ns

(1) to all inputs, (2) Fan out = 10, (3) Fan out = 20

(4) Only one output at a time, duration $t < 1 \text{ sec}$

* See 3.2.1. of this specification

CHARACTERISTICS	CONDITIONS	V _{CC} (V)	SYMBOL	MIN.	MAX.	UNIT
Propagation times (Cont'd)						
$\overline{CS}$, R/ $\overline{W}$ $\rightarrow$ SER/Q15			t _{PZH}	-	45.0	ns
			t _{PZL}	-	45.0	ns
$\overline{CS}$, R/ $\overline{W}$ $\rightarrow$ SER/Q15			t _{PHZ}	-	40.0	ns
			t _{PLZ}	-	40.0	ns
Set-up time						
SER/Q15			tpset-up	20.0	-	ns
MODE			tpset-up	35.0	-	ns
R/ $\overline{W}$, $\overline{CS}$			tpset-up	35.0	-	ns
Hold time						
SER/Q15			tphold	0	-	ns
MODE			tphold	0	-	ns