

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

SPECIFICATION AVAILABLE FROM:- As shown in PD 9002
AND CECC 00 200 ANDTEXAS INSTRUMENTS LIMITED,
MANTON LANE,
BEDFORD, MK41 7PA

BS CECC 90103-181

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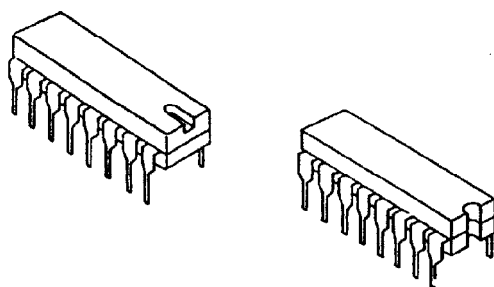
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ELECTRONIC COMPONENTS OF ASSESSED QUALITY

DETAIL SPECIFICATION IN ACCORDANCE WITH:-

BS CECC 90 000 : 1976

BS CECC 90 100 : 1977

Outline not to scale. Isometric projection
Marking information see Clause 1

For detail dimensions: BS 3934 S0-87C

MANUFACTURERS TYPE NUMBER

54LS375

64LS375

74LS375

84LS375

SEE PD 9002 AND CECC 00 200
For ordering information
see Clause 1

4-BIT BISTABLE LATCHES

TYPICAL CONSTRUCTION SILICON
MONOLITHIC BIPOLAR LOW-
POWER SCHOTTKY TTLASSESSMENT LEVELS R, S, T
AND V1. TYPE DESCRIPTION

1.1. Truth table (see Page 2)

REFER TO QUALIFIED PRODUCTS LIST PD 9002 AND/OR CECC 00 200
FOR DETAILS OF MANUFACTURERS APPROVED TO THIS SPECIFICATION

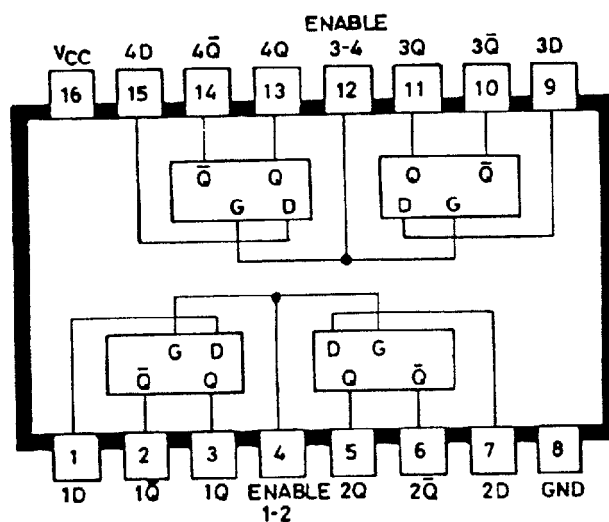
1.1. Truth Table (cont'd)
(each bistable latch)

INPUTS		OUTPUTS	
D	G	Q	$\bar{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\bar{Q}_0$

H = High level
L = Low level
X = Logic level irrelevant
 $Q_0, \bar{Q}_0$ = The level of Q and $\bar{Q}$ before the indicated steady level input conditions.

1.2. Terminal identification, type designation and marking

1.2.1. Terminal identification



4-Bit Bistable Latches

1.2.2 Type designation

TEMPERATURE RANGE	PACKAGE		
	Ceramic Dual-in-Line	Plastic Dual-in-Line	Ceramic Flatpack
0 + 70	74LS375J	N	W
-25 + 85	84LS375J		
-40 + 85	64LS375J		
-55 +125	54LS375J		

1.2.3 Marking

Each integrated circuit shall bear the following markings:

- (1) Terminal identification
- (2) Type designation
- (3) Date code
- (4) Factory identification code (unless derived from trademark)
- (5) Manufacturers trade name or mark
- (6) Mark of conformity (unless a certificate of conformity is used)

1.3 Ordering information

Orders for these integrated circuits shall contain the following minimum information:

Manufacturers integrated circuit type designation, screening procedures and assessment levels as detailed to this CECC specification number.

(For details of screening procedures see Appendix A1.1)

2. Limiting conditions of use (not for inspection purposes)

2.1	Maximum continuous supply voltage	V_{CC}					-0,5V +7,0V
2.2	Maximum input voltages						
2.2.1	Maximum input voltage	V_I					-0,5V +7,0V
2.2.2	Maximum input voltage between multiple emitter transistor inputs	V_{II}					+5,5V
2.3	Minimum and maximum operating ambient temperatures	$T_{amb}(^{\circ}C)$	min.	54LS -55	64LS -40	74LS 0	84LS -25
			max.	+125	+85	+70	+85
2.4	Minimum and maximum storage temperatures	$T_{stg}(^{\circ}C)$	min.	-65	(All types)		
			max.	+150			

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3. Recommended operating conditions and associated characteristics (not for inspection purposes)

3.1 Recommended operating conditions.

These apply over the operating ambient temperature range unless otherwise stated.

Description	Symbol	Type	Value	Unit
Positive supply voltage range	V_{CC}	54LS 64/74/84LS	4,5 - 5,5 4,75 - 5,25	V V
Minimum value of High level input voltage	V_{IHB}	All types	2,0	V
Maximum value of High level input voltage	V_{IHA}	All types	5,5	V
Minimum value of Low level input voltage	V_{ILB}	All types	-0,3	V
Maximum value of Low level input voltage	V_{ILA}	54LS 64/74/84LS	0,7 0,8	V V
Maximum value of Low level output current for each output	I_{OLA}	54LS 64/74/84LS	4,0 8,0	mA mA
Maximum value of output current for each output at V_{OH}	I_{OHA}	All types	-400,0	μA
D.C. noise margin at Low level ($V_{ILA} - V_{OLA}$)	V_{NL}	All types	0,3	V
at High level ($V_{OHB} - V_{IHB}$)	V_{NH}	54LS 64/74/84LS	0,5 0,7	V V

3.2 Associated characteristics

- 3.2.1 Minimum and maximum values are given for the worst case operation over the ambient temperature range, except for those conditions marked with an asterisk (*)

3.2.1 (contd)

	54LS	64LS	74LS	84LS	
T _{amb} min.	-55	-40	0	-25	°C
T _{amb} max.	+125	+85	+70	+85	
V _{CC} min.	4,5	4,75			V
V _{CC} max.	5,5	5,25			

3.2.2

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Total supply current per package	0V to all inputs Outputs open circuit	V_{CC} max.	I_{CC}	-	12,0	mA
High level input current	$V_{IH(1)} = 7,0V$	V_{CC} max.				
	D input		$I_{IH(1)}$	-	0,1	mA
	G input		$I_{IH(1)}$	-	0,4	mA
	$V_{IH(2)} = V_{OHB}$					
Low level input current	D input	V_{CC} max.	$I_{IH(2)}$	-	20,0	µA
	G input		$I_{IH(2)}$	-	80,0	µA
	$V_{IL} = 0,4V$ to each input in turn					
	D input		$-I_{IL}$	-	0,4	mA
Input clamping voltage	G input	V_{CC} min.	$-I_{IL}$	-	1,6	mA
	$-I_{IC} = 18,0mA$		$-V_{ICA}$	-	1,5	V

3.2.2 (contd)

Characteristics	Conditions	$V_{CC}(V)$	Symbol	Min.	Max.	Unit
Output voltage	$V_{IN} = V_{ILA}$ or 2,0V as appropriate. Test each output in turn.	V_{CC} min.				
54LS	$I_{OH} = -400,0\mu A$		V_{OH}	2,5	-	V
64/74/84LS	$I_{OH} = -400,0\mu A$		V_{OH}	2,7	-	V
All types	$I_{OL(1)} = 4,0mA$ (1)		$V_{OL(1)}$	-	0,4	V
64/74/84LS	$I_{OL(2)} = 8,0mA$ (2)		$V_{OL(2)}$	-	0,5	V
Output short circuit current	$V_{IN} = 0V$ or 4,5V as appropriate $V_O = 0V$ (3)	V_{CC} max.	$-I_{OS}$	15,0	130,0	mA
Propagation times	$T_{amb} = 25^{\circ}C^*$ test conditions as in Sub-group A5	5,0V				
All types						
High to Low level	<u>From</u> <u>To</u>					
	D Q		t_{PHL}	-	17,0	ns
	D $\overline{Q}$		t_{PHL}	-	15,0	ns
	G Q		t_{PHL}	-	25,0	ns
	G $\overline{Q}$		t_{PHL}	-	15,0	ns
Low to High level	<u>From</u> <u>To</u>					
	D Q		t_{PLH}	-	27,0	ns
	D $\overline{Q}$		t_{PLH}	-	20,0	ns
	G Q		t_{PLH}	-	27,0	ns
	G $\overline{Q}$		t_{PLH}	-	30,0	ns
Set-up time			t_{set-up}	20,0	-	ns
Duration of Enable pulse			t_p (enable)	20,0	-	ns
Hold time			t_{hold}	5,0	-	ns

(1) Fan out = 10, (2) Fan out = 20,

(3) Only one output at a time, duration $t \leq 1$ sec

*See 3.2.1 of this specification