

Förderverein für Elektrotechnische Normung (FEN) e. V.
Cenelec Electronic Components Committee

CECC

Système Harmonisé d'Assurance de la Qualité
des Composants Electroniques

SPECIFICATION DE FAMILLE:

**CIRCUITS INTEGRES
DIGITAUX TTL
LOW POWER SCHOTTKY**
Séries 54 LS, 64 LS, 74 LS, 84 LS

Harmonized System of Quality Assessment for
Electronic Components

FAMILY SPECIFICATION:

**DIGITAL INTEGRATED
TTL LOW POWER
SCHOTTKY CIRCUITS**
Sieres L4 5S, 64 LS, 74 LS, 84 LS

Harmonisiertes Gütebestätigungssystem für
Bauelemente der Elektronik

FAMILIEN-SPEZIFIKATION:

**DIGITALE INTEGRIERTE
TTL LOW POWER
SCHOTTKY-
SCHALTUNGEN**
Serien 54 LS, 64 LS, 74 LS, 84 LS



3

Edition
Issue
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Documents



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Information about the System may be obtained from:



FEN Secretariat
and
CECC General Secretariat
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Telefax Int.+ (49) 69 6 30 82 83 (Gr. 2/3)
or from the National Authorized Institutions
of the participating countries listed
who can supply copies of:

- 1 The Internal Regulations of the FEN e.V.
- 2 CECC Specifications of the FEN and National Specifications for the System
- 3 CECC 00 200: Qualified Products List (QPL)
- 4 CECC 00 300: CECC Publications and their related national documents

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Finnish Electrotechnical
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S-16428 Kista-Stockholm

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CH- 8008 Zürich

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FOREWORD

The CENELEC Electronic Components Committee (CECC) is composed of those member countries of the European Committee for Electrotechnical Standardization (CENELEC) who wish to take part in a harmonized System for electronic components of assessed quality.

The object of the System is to facilitate international trade by the harmonization of the specifications and quality assessment procedures for electronic components, and by the grant of an internationally recognized Mark, or Certificate, of Conformity. The components produced under the System are thereby accepted by all member countries without further testing.

This specification has been formally approved by the CECC, and has been prepared for those countries taking part in the System who wish to issue national harmonized specifications for TTL LOW POWER SCHOTTKY DIGITAL INTEGRATED CIRCUITS. It should be read in conjunction with the current regulations for the CECC System.

At the date of printing of this specification the member countries of the CECC are Austria, Belgium, Denmark, Finland, France, Germany, Ireland, Italy, the Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom, and copies of it can be obtained from the addresses shown on the blue fly sheet.

PREFACE

This Family Specification was prepared by CECC WG9 "INTEGRATED CIRCUITS".

It is based, wherever possible, on the Publications of the International Electrotechnical Commission and in particular on IEC 747 : Semiconductor devices : Discrete devices and integrated circuits, IEC 748 : Semiconductor devices : Integrated circuits, IEC 749 : Semiconductor devices : Mechanical and climatic test methods.

It contains general information on TTL Low Power Schottky digital integrated circuits and defines the common characteristics for this family of integrated circuits.

Together with the device type detail specification (DS) of a component usually prepared nationally, this family specification forms a complete detail specification.

The text of this third Issue consists of the text of CECC 90 103 Issue 2 (1982) amended in accordance with the ratified new material introduced by the following document.

<u>Document</u>	<u>Date of Voting</u>	<u>Report on the Voting</u>
CECC(Secretariat)2094	July 1987	CECC(Secretariat)2162

In accordance with the decision of the CECC Management Committee this specification is published initially in French and English. The German text will follow as soon as it has been prepared.

EFFECTIVE DATE

This third Issue of CECC 90 103 shall become effective for all new qualification approvals on 15 June 1988. Issue 2 will continue to remain effective to cover all past approvals.

CECC 90 103

ISSUE 3 - 1988



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Total number of pages : 20

**ELECTRONIC COMPONENTS OF ASSESSED QUALITY
IN ACCORDANCE WITH :**

CECC 90 000 : Generic specification for
Monolithic integrated circuits (GS)
CECC 90 100 : Sectional specification for
Digital monolithic integrated circuits (SS)

OUTLINE AND DIMENSIONS :
(See DS for the specific type)

TERMINAL CONNECTIONS
(See DS for the specific type)

**FAMILY SPECIFICATION FOR
TTL LOW POWER SCHOTTKY
DIGITAL INTEGRATED CIRCUITS**
Category 1 : Usual series 54 LS, 64 LS, 74 LS, 84 LS

Category 2 : Harmonized series 54 LS, 74 LS

*NOTE : This family specification shall be completed
by a DS in accordance with this specification covering
one or more specific types of circuits. The marking
shall differentiate the Category 1 components from
Category 2 components.*

TYPICAL CONSTRUCTION :

Silicon monolithic bipolar integrated circuits, cavity/
non-cavity packages.

CAUTION : These are electrostatic sensitive devices.

ASSESSMENT LEVELS : P, Y, L

CONTENTS
CATEGORY 1 - (USUAL 54 LS, 64 LS, 74 LS, 84 LS)

- 1 - LIMITING CONDITIONS OF USE FOR THE FAMILY
- 2 - RECOMMENDED OPERATING CONDITIONS AND ASSOCIATED CHARACTERISTICS
FOR THE FAMILY

CATEGORY 2 - (HARMONIZED 54 LS, 74 LS)

- 3 - LIMITING CONDITIONS OF USE FOR THE FAMILY
- 4 - RECOMMENDED OPERATING CONDITIONS AND ASSOCIATED CHARACTERISTICS
FOR THE FAMILY

CATEGORIES 1 AND 2

- 5 - TEST METHODS AND PROCEDURES
- 6 - INSPECTION REQUIREMENTS

Information about manufacturers who have components qualified to a detail specification written in accordance
with this family specification is available in the current CECC 00 200 : Qualified Products List.

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**Documents**

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CATEGORY 1 (USUAL SERIES 54 LS, 64 LS, 74 LS, 84 LS)

1 LIMITING CONDITIONS OF USE FOR THE FAMILY (Not for inspection purpose)

1.1 Maximum continuous supply voltage

$$V_{CC} : -0,5 \text{ V} \\ + 7,0 \text{ V}$$

1.2 Maximum input voltages

1.2.1 Max. input voltage

$$V_I : -0,5 \text{ V} \\ + 7,0 \text{ V}$$

1.2.2 Max. input voltage between multiple emitter transistor inputs

$$V_{II} : + 5,5 \text{ V}$$

1.3 Minimum and maximum operating ambient temperatures

T_{amb} (°C)	54 LS	64 LS	74 LS	84 LS
min.	- 55	- 40	0	- 25
max.	+ 125	+ 85	+ 70	+ 85

1.4 Minimum and maximum storage temperatures

$$T_{stg} : \begin{matrix} - 65 \text{ °C min.} \\ + 150 \text{ °C max.} \end{matrix} \quad \left. \vphantom{\begin{matrix} - 65 \text{ °C min.} \\ + 150 \text{ °C max.} \end{matrix}} \right\} \text{ (unless otherwise specified in the DS)}$$

2 RECOMMENDED OPERATING CONDITIONS AND ASSOCIATED CHARACTERISTICS FOR THE FAMILY (Not for inspection purpose)

(See also relevant DS)

These conditions apply to the total operating temperature range, unless otherwise prescribed.

2.1 Positive supply voltage

$$V_{CC} : 4,5 \text{ to } 5,5 \text{ V (54 LS)} \\ 4,75 \text{ to } 5,25 \text{ V (64 LS, 74 LS, 84 LS)}$$

2.2 Most negative low level input voltage at an input current $I_{IK} = -18 \text{ mA}$

$$V_{IKB} : -1,5 \text{ V}$$

2.3 Minimum low level input voltage

$$V_{ILB} : 0 \text{ V}$$

2.4 Maximum low level input voltage

$$V_{ILA} : 0,7 \text{ V (54 LS)} \\ 0,8 \text{ V (64 LS, 74 LS, 84 LS)}$$

- 2.5 Minimum high level input voltage

$V_{IHB} : 2 \text{ V}$

- 2.6 Maximum high level input voltage

$V_{IHA} : 5,5 \text{ V}$

- 2.7 Most positive low level output voltage at an output current of 0,4 mA x the higher fanout (unless otherwise prescribed in the DS)

$V_{OLA} : 0,4 \text{ V (54 LS)}$
 $0,5 \text{ V (64 LS, 74 LS, 84 LS)}$

- 2.8 Most negative high level output voltage at an output current of $-20 \mu\text{A}$ x the higher fanout

$V_{OHB} : 2,5 \text{ V (54 LS)}$
 $2,7 \text{ V (64 LS, 74 LS, 84 LS)}$

- 2.9 Most positive high level output voltage

$V_{OHA} : 5,5 \text{ V (54 LS)}$
 $5,25 \text{ V (64 LS, 74 LS, 84 LS)}$

- 2.10 DC noise margin at low level ($V_{ILA} - V_{OLA}$)

$V_{NL} : 0,3 \text{ V}$

- 2.11 DC noise margin at high level ($V_{OHB} - V_{IHB}$)

$V_{NH} : 0,5 \text{ V (54 LS)}$
 $0,7 \text{ V (64 LS, 74 LS, 84 LS)}$

CATEGORY 2 (HARMONIZED SERIES 54 LS, 74 LS)

3 LIMITING CONDITIONS OF USE FOR THE FAMILY (Not for inspection purpose)

3.1 Maximum continuous supply voltage

$$V_{CC} : -0,5 \text{ V} \\ + 7,0 \text{ V}$$

3.2 Maximum input voltages

3.2.1 Max. input voltage

$$V_I : -0,5 \text{ V} \\ + 7,0 \text{ V}$$

3.2.2 Max. input voltage between multiple emitter transistor inputs

$$V_{II} : + 5,5 \text{ V}$$

3.3 Minimum and maximum operating ambient temperatures

T_{amb} (°C)	54 LS	74 LS
min.	- 55	0
max.	+ 125	+ 70

3.4 Minimum and maximum storage temperatures

$$T_{stg} : \begin{matrix} - 65 \text{ °C min.} \\ + 150 \text{ °C max.} \end{matrix} \quad \left. \vphantom{\begin{matrix} - 65 \text{ °C min.} \\ + 150 \text{ °C max.} \end{matrix}} \right\} \text{ (unless otherwise specified in the DS)}$$

4 RECOMMENDED OPERATING CONDITIONS AND ASSOCIATED CHARACTERISTICS FOR THE FAMILY (Not for inspection purposes)

(See also relevant DS)

These conditions apply to the total operating temperature range, unless otherwise prescribed.

4.1 Positive supply voltage

$$V_{CC} : 4,5 \text{ to } 5,5 \text{ V}$$

4.2 Most negative low level input voltage at an input current $I_{IK} = -18 \text{ mA}$

$$V_{IKB} : -1,5 \text{ V}$$

4.3 Minimum low level input voltage

$$V_{ILB} : 0 \text{ V}$$

4.4 Maximum low level input voltage

$$V_{ILA} : 0,8 \text{ V } (T_{amb} \leq + 70 \text{ °C}) \\ 0,7 \text{ V } (+ 70 \text{ °C} < T_{amb} \leq + 125 \text{ °C})$$

4.5 Minimum high level input voltage

$$V_{IHB} : 2 \text{ V}$$

4.6 Maximum high level input voltage

$$V_{IHA} : 5,5 \text{ V}$$

4.7 Load factors

4.7.1 Unit load current

(1) At low level voltage : 0,4 mA

(2) At high level voltage : - 10 μ A

4.7.2 Input load factor (fan-in)

(1) At low level input voltage
(2) At high level input voltage } (see DS for the relevant input)

4.7.3 Output loading capability (fan-out)

(1) At low level output voltage
(2) At high level output voltage } (see DS for the relevant output)

4.8 Most positive low level output voltages

4.8.1 With a maximum fanout (see 4.7.3 (1))

$$V_{OLA(1)} : 0,45 \text{ V}$$

4.8.2 With an output current corresponding at 1,5625 times the maximum fanout (see 4.7.3 (2)) (unless otherwise prescribed in the DS)

$$V_{OLA(2)} : 0,8 \text{ V } (0^\circ\text{C} \leq T_{\text{amb}} \leq + 125^\circ\text{C})$$

4.9 Most negative high level output voltage at an output current corresponding to the maximum fanout

$$V_{OHB} : 2,5 \text{ V}$$

4.10 Most positive high level output voltage

$$V_{OHA} : 5,5 \text{ V}$$

4.11 DC noise margin at low level ($V_{ILA} - V_{OLA(1)}$)

$$V_{NL} : 0,35 \text{ V } (T_{\text{amb}} \leq + 70^\circ\text{C})$$

$$0,25 \text{ V } (+ 70^\circ\text{C} < T_{\text{amb}} \leq + 125^\circ\text{C})$$

4.12 DC noise margin at high level ($V_{OHB} - V_{IHB}$)

$$V_{NH} : 0,5 \text{ V}$$

CATEGORIES 1 AND 2

5 TEST METHODS AND PROCEDURES

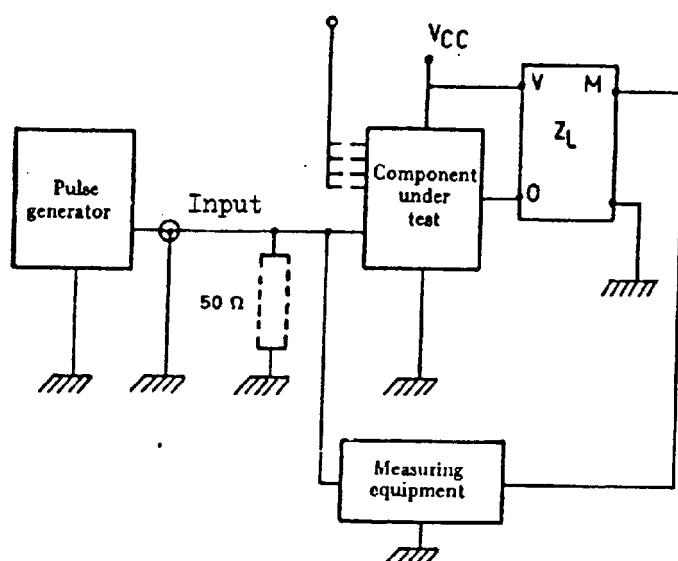
5.1 Dynamic characteristics

Unless otherwise prescribed in the relevant DS, the following dynamic measurement conditions are applicable.

5.1.1 General diagram

Measurements of dynamic characteristics are performed in accordance with the general diagram of figure 1.

Inputs (according to the test to be performed, see relevant DS)



Z_L = Load circuit :
according to the output
configuration given in the DS,
the load circuit diagram
A, B or C shown below
(see 5.1.4) is applicable.

FIG. 1 - DIAGRAM FOR SWITCHING PARAMETERS

NOTES : 1 - The inductances of the connections and of the components used, and the impedance of the continuous sources shall be so low as to make the error negligible.

2 - One or more pulse generators may be used according to the measurement to be performed.

5.1.2 Pulse generator and driving circuit

The following conditions shall be met :

- output impedance of pulse generator : $50\ \Omega \pm 10\ \%$
- impedance of the driving circuit cable from the generator, including the test equipment : $50\ \Omega \pm 10\ \%$

Signal applied to the inputs of the component under test (see figure 2).

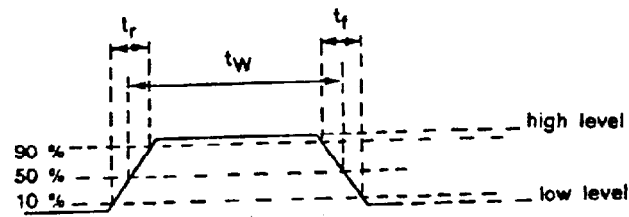


FIG. 2 - SIGNAL WAVEFORM AT THE INPUT OF THE COMPONENT UNDER TEST

Low level input voltage : $0 \text{ V} \pm 0,1 \text{ V}$

High level input voltage : $3 \text{ V} \pm 0,2 \text{ V}$

Rise time of the input signal : $t_r = 15 \text{ ns} \pm 1 \text{ ns}$
(measured from 10 % to 90 % of the step amplitude)

Fall time of the input signal : $t_f = 6 \text{ ns} \pm 1 \text{ ns}$
(measured from 90 % to 10 % of the step amplitude)

Pulse width : $t_W = 0,5 \mu\text{s}$

Pulse repetition frequency : $\leq 1 \text{ MHz}$

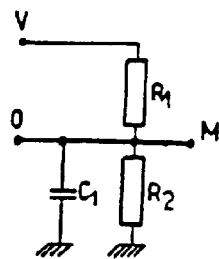
5.1.3 Component under test

- load circuit : (see 5.1.4)
- untested input(s) of the component under test are biased according to the characteristics to be tested (see DS)
- power supply $V_{CC} = 5 \text{ V}$
- for multiple devices the inputs of circuit(s) not under test shall be left unconnected
- reference point for time measurements shall be taken according to the following :
 - passive load circuit : 1,4 V
 - active load circuit : 1,3 V

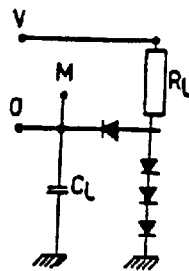
5.1.4 Load circuit

- in accordance with figure 1 (see 5.1.1)
- capacitances and resistances include probe and jig capacitance and resistance
- for Category 1 : the DS prescribes the load circuit(s)
- for Category 2 : measurements can be performed with either active or passive load circuits without ranking. If the two results do not correlate, the passive load circuit is used as a reference.

A - Load circuits for totem pole outputs



$$\begin{aligned} R_1 &= 1\,150\,\Omega \\ R_2 &= 3\,010\,\Omega \\ C_1 &= 50\,\text{pF} \end{aligned}$$

CIRCUIT A1 (PASSIVE)
(Category 2 only)

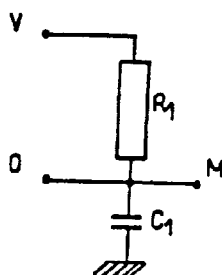
Diodes
1 N 3064
or equivalent

	Standard outputs A2	Buffer outputs A3
$R_L (\Omega)$	2 000	667
$C_L (\text{pF})$	15	45

CIRCUITS A2 AND A3 (ACTIVE)

NOTE: R_L and C_L may be different from values given in the above table. In this case see DS.

B - Load circuit for open-collector outputs



	Standard outputs B1	Buffers outputs B2
$R_1 (\Omega)$	2 000	667
$C_1 (\text{pF})$	15	45

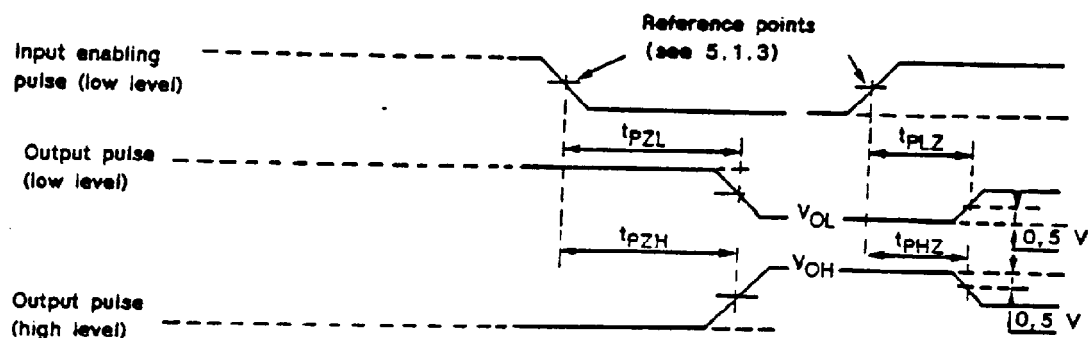
No active load circuit is specified for this output configuration

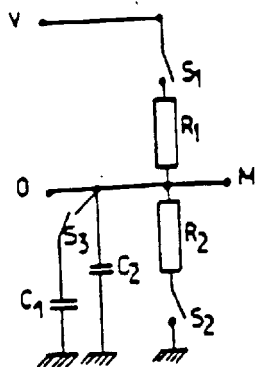
CIRCUITS B1 AND B2
(PASSIVE)

NOTE: R_1 and C_1 may be different from values given in the above table. In this case see DS.

C - Load circuit for three-state outputs

Observed waveforms





$$R_1 = 1\,150\,\Omega$$

$$R_2 = 3\,010\,\Omega$$

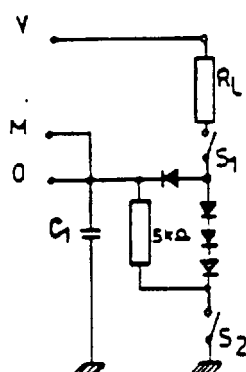
$$C_1 = 35\,\text{pF}$$

$$C_2 = 15\,\text{pF}$$

PARAMETER	S ₁	S ₂	S ₃
t _{PHL}	C	C	C
t _{PLH}	C	C	C
t _{PZL}	C	O	C
t _{PZH}	O	C	C
t _{PLZ}	C	O	O
t _{PHZ}	O	C	O

CIRCUIT C1 (PASSIVE)
(Category 2 only)

O : Open C : Closed



Diodes 1 N 3064
or equivalent

PARAMETER	S ₁	S ₂	Standard outputs C2		Buffer outputs C3	
			R _L (Ω)	C _L (pF)	R _L (Ω)	C _L (pF)
t _{PHL}	C	C	2 000	15	667	45
t _{PLH}	C	C	2 000	15	667	45
t _{PZL}	C	O	2 000	15	667	45
t _{PZH}	O	C	2 000	15	667	45
t _{PLZ}	C	C	2 000	5	667	5
t _{PHZ}	C	C	2 000	5	667	5

CIRCUITS C2 AND C3
(ACTIVE)

NOTE: R_L and C_L values may be different from
the values given above. In this case see DS.

5.1.5 Transition and delay times

For Category 2 only.

The transition times and the delay times, specified in clause 5 of the DS will be verified in Sub-Group C15 according to the limits prescribed in the relevant DS.

5.2 Conditions for the electrical endurance tests

For Category 1 and Category 2.

See SS/4.2.2

Unless otherwise specified in the relevant DS, the inputs are biased for the highest I_{CC} .

Maximum output loading capability is applied (I_{OH} or I_{OL} according to high or low level conditions).

If the temperature limits of the device are exceeded, the DS shall prescribe the relevant test conditions (see SS/4.2).

6 INSPECTION REQUIREMENTS

For Category 1 and Category 2.

These requirements are given in the following tables and in the relevant DS.

NOTES : 1 - All tests are performed at $T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise prescribed.

2 - In the tables the clause numbers refer to the generic, to the sectional or to this family specification with the following code :

GS : Generic Specification (CECC 90 000, Issue 3)

SS : Sectional Specification (CECC 90 100, Issue 3)

FS : Family Specification (CECC 90 103, Issue 3)

Example : GS/4.2.2 = 4.2.2 of CECC 90 000.

3 - The following abbreviations are used :

D : destructive test

ND : non-destructive test

IL : inspection level

AQL : acceptable quality level

n : sample size

c : acceptance criterion

na : not applicable

EXAMINATION OR TEST	D ND	CONDITIONS OF TEST	LIMITS TO BE SPECIFIED	INSPECTION REQUIREMENTS					
GROUP A INSPECTION : The following electrical inspection requirements shall be given. Additional characteristics to be inspected may be given for the specific circuit(s) in accordance with SS/5.3.8. The tests of group A can be done totally or partly on the same sample, by applying the tightest IL and AQL. A circuit is considered defective with appearance of the first defect.				ASSESSMENT LEVELS					
				P (Note 1)		Y (Note 2)		L (Note 2)	
				IL	AQL	IL	AQL	IL	AQL
<u>Sub-Group A0</u> Internal visual examination (before encapsulation)	ND	GS/Annex A (Condition B, unless otherwise specified)		S4	2,5	na	na	na	na
<u>Sub-Group A1</u> External visual examination GS/4.2.2	ND	GS/4.2.2	External visual examination (visual) inoperatives (Note 3)	II	0,1	II	0,65	II	0,65
<u>Sub-Group A2</u> Verification of the function at 25 °C (Note 4) SS/4.1.1	ND	Supply voltage(s)	The output signals as function of input signals shall be verified	II	0,1	II	0,1	II	0,25
<u>Sub-Group A3</u> Static characteristics at 25 °C SS/5.5.1	ND	See relevant DS	See relevant DS	A2 + A3 + A5 II	0,25	II	0,25	II	0,65
<u>Sub-Group A4a</u> Static characteristics at maximum operating temperature As in Sub-Group A3	ND	T _{amb} = T _{amb} max. Electrical conditions as for Sub-Group A3	See relevant DS Limits may be dif- ferent from those in Sub-Group A3	n 80	c 1 A4a + A4b + A6a + A6b + A7a + A7b	S4	0,65	S4	1,5
<u>Sub-Group A4b</u> Static characteristics at minimum operating temperature As in Sub-Group A3	ND	T _{amb} = T _{amb} min. Electrical conditions as for Sub-Group A3	See relevant DS Limits may be dif- ferent from those in Sub-Group A3			II	0,25 see note 5	II	0,65 see note 5

Notes :

- One inspection lot : max. 1 week and max. 35 000 devices.
- One inspection lot : max. 1 month or 4 consecutive weeks.
- Only the following defects are defined as (visual) inoperatives :
 - type identification marking, missing or wrong
 - wrong reference for terminal identification
 - pins missing and/or broken
 - package damaged or incomplete such that chip or bond wires are exposed
- Verification of the function may be implicitly contained in tests performed in Sub-Groups A3 to A7b.
- Correlated measurements are allowed (procedure under consideration)