

NEDERLANDS ELEKTROTECHNISCH
COMITE
POSTBOX 5059
2600 GB DELFT

This specification is also available from
Nederlandse Philips Bedrijven B.V.

CECC 90 104-026

ISSUE 3



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Total number of pages: 16

ELECTRONIC COMPONENTS OF ASSESSED
QUALITY IN ACCORDANCE WITH:

GS: CECC 90 000 Issue 3.

SS: CECC 90 100 Issue 3.

FS: CECC 90 104 Issue 2.

Detail Spec: NL-CECC 90 104-026

Issue: 3

Issued: August 1990

OUTLINE AND DIMENSIONS:

IEC 191-2 | 050 G09/A76 G1

TERMINAL CONNECTIONS:

See item 1.3 of this specification

DETAIL SPECIFICATION FOR
DIGITAL INTEGRATED CIRCUITS
IN ACCORDANCE WITH FS 90 104

HEC/HEF 4029B

Synchronous up/down counter,
binary/decade counter

TYPICAL CONSTRUCTION:

Silicon monolithic local oxidation
CMOS integrated circuit, cavity/non-
cavity packages.

CAUTION: STATIC SENSITIVE DEVICE

ASSESSMENT LEVELS: P, Y, L

REMARKS

Information about manufacturers who have components qualified to this detail specification is
available in the current CECC 00 200: Qualified Products List.



Documents

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1 TYPE DESCRIPTION

1.1 Function

The HEC/HEF4029B are synchronous edge-triggered up/down 4-bit binary/BCD decade counters with a clock input (CP), an active LOW count enable input ($\overline{CE}$), an up/down control input (UP/ $\overline{DN}$), a binary/decade control input (BIN/ $\overline{DEC}$), an overriding asynchronous active HIGH parallel load input (PL), four parallel data inputs (P_0 to P_3), four parallel buffered outputs (O_0 to O_3) and an active LOW terminal count output ($\overline{TC}$).

Information on P_0 to P_3 is asynchronously loaded into the counter while PL is HIGH, independent of CP.

The counters are advanced one count on the LOW to HIGH transition of CP when $\overline{CE}$ and PL are LOW. The $\overline{TC}$ signal is normally HIGH and goes LOW when the counters reach their maximum count in the UP mode, or the minimum count in the DOWN mode provided $\overline{CE}$ is LOW.

1.1.1 Function table

PL	BIN/ $\overline{DEC}$	UP/ $\overline{DN}$	$\overline{CE}$	CP	mode
H	X	X	X	X	parallel load ($P_n \rightarrow O_n$)
L	X	X	H	X	no change
L	L	L	L	$\nearrow$	count-down, decade
L	L	H	L	$\nearrow$	count-up, decade
L	H	L	L	$\nearrow$	count-down, binary
L	H	H	L	$\nearrow$	count-up, binary

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

$\nearrow$ = positive-going clock pulse edge

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1.1.2 State diagrams

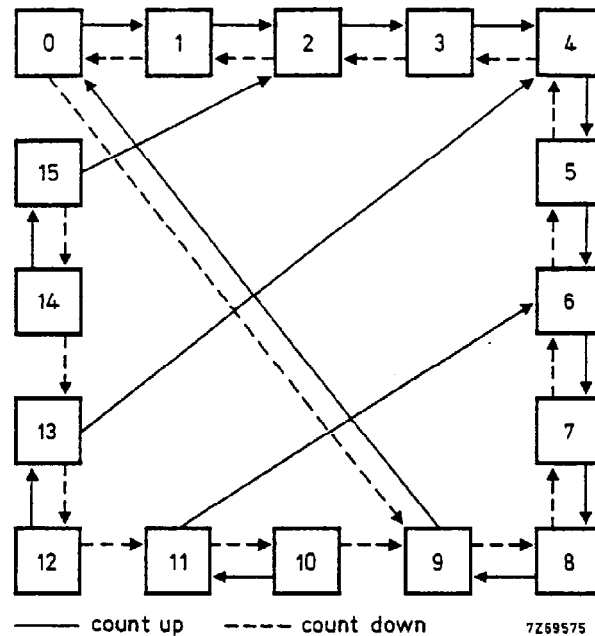


Fig. 1 State diagram; BIN/DEC = LOW.

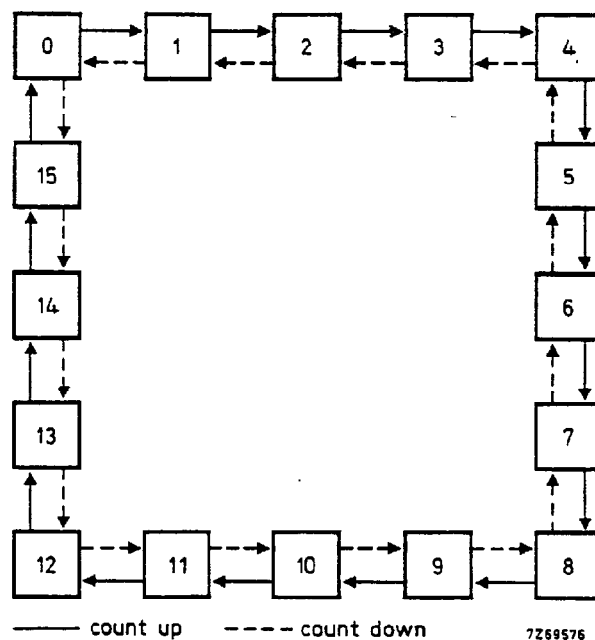


Fig. 2 State diagram; BIN/DEC = HIGH.

Logic equation for terminal count:

$$TC = \overline{CE} (\overline{BIN/DEC} \cdot \overline{UP/DN} \cdot O_0 \cdot O_1 \cdot O_2 \cdot O_3 + \overline{BIN/DEC} \cdot \overline{UP/DN} \cdot \overline{O_0} \cdot \overline{O_1} \cdot \overline{O_2} \cdot \overline{O_3} + \overline{BIN/DEC} \cdot \overline{UP/DN} \cdot O_0 \cdot O_3 + \overline{BIN/DEC} \cdot \overline{UP/DN} \cdot \overline{O_0} \cdot \overline{O_1} \cdot \overline{O_2} \cdot \overline{O_3})$$



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1.1.3 Functional diagram

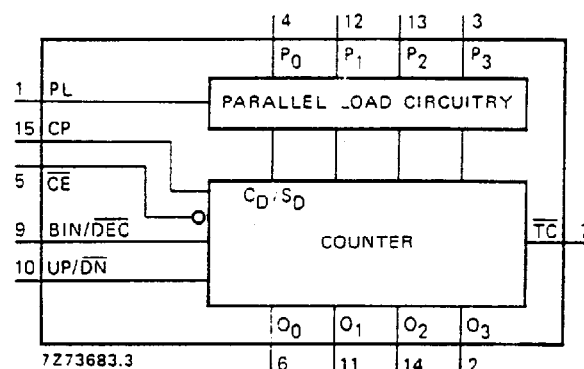


Fig. 3 Functional diagram.

1.1.4 Pinning information

PL	parallel load input
P ₀ to P ₃	parallel data inputs
BIN/ $\overline{\text{DEC}}$	binary/decade control input
UP/ $\overline{\text{DN}}$	up/down control input
$\overline{\text{CE}}$	count enable input (active LOW)
CP	clock input (LOW to HIGH, edge triggered)
O ₀ to O ₃	buffered parallel outputs
$\overline{\text{TC}}$	terminal count output (active LOW)

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1.2 Logic diagram

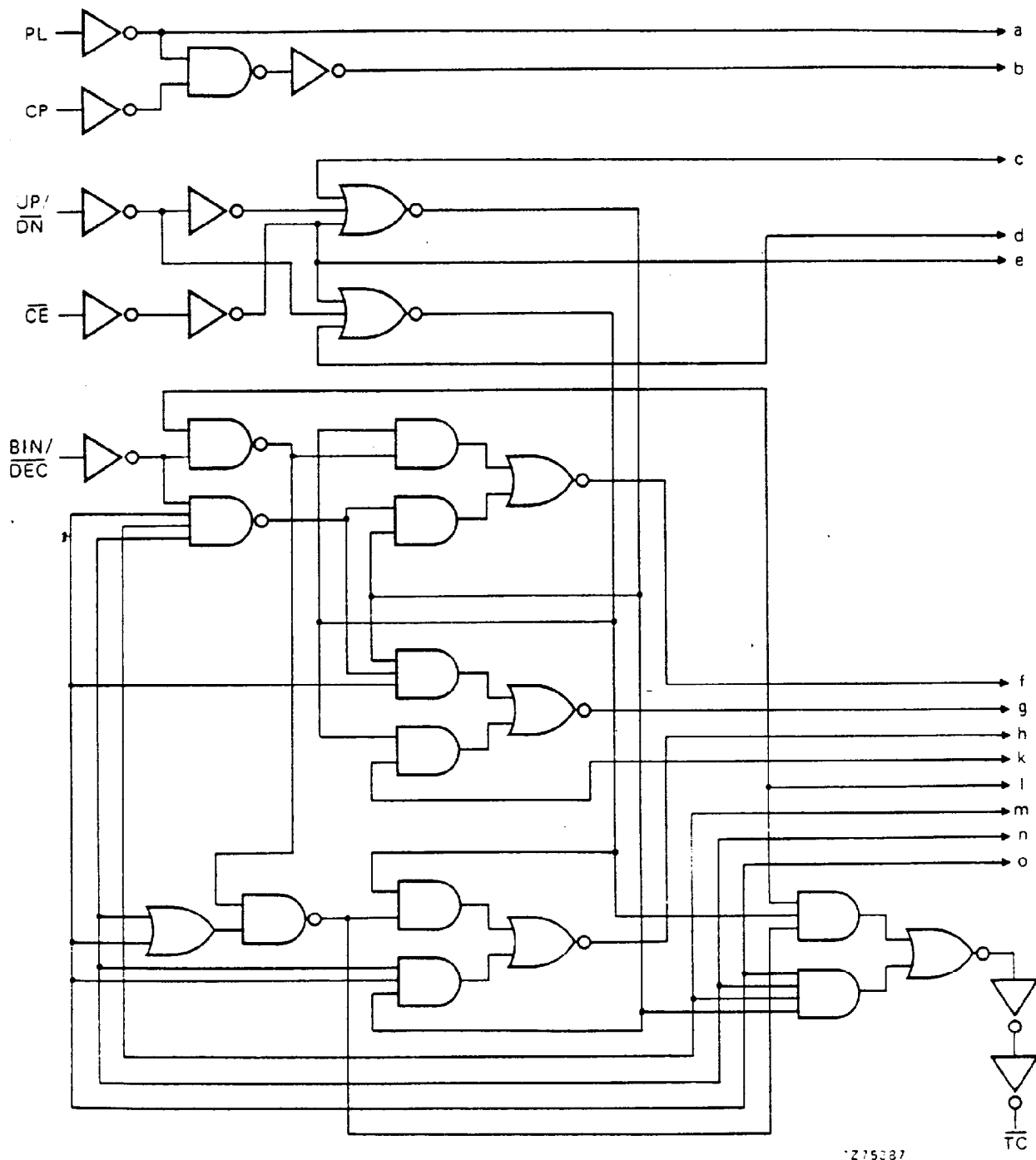


Fig. 4a Logic diagram (continued in Fig. 4b).