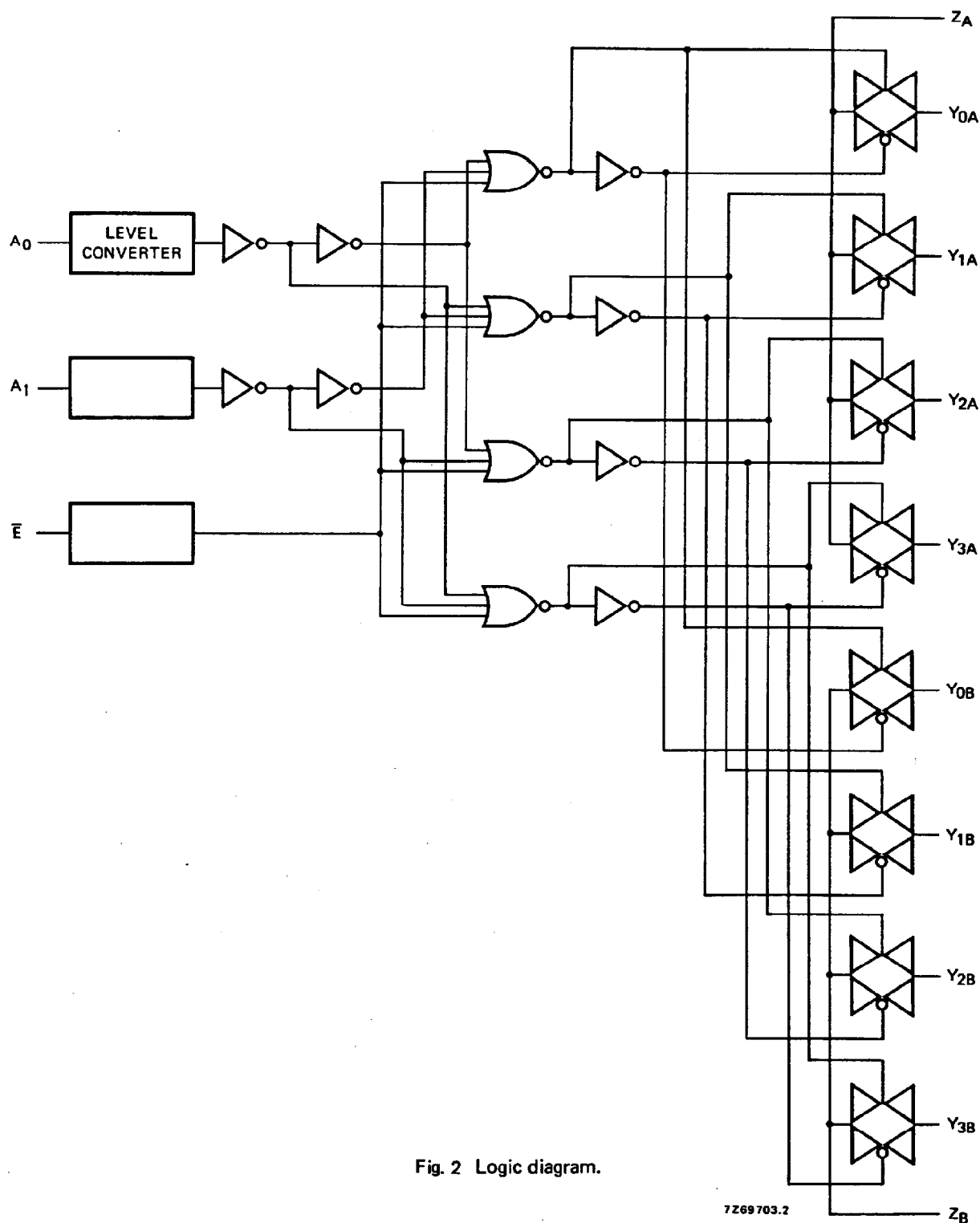


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ELECTRONIC COMPONENT OF ASSESSED QUALITY IN ACCORDANCE WITH NEN-CECC 90 000 ISSUE 2 1982 NEN-CECC 90 100 ISSUE 2 1983	DETAIL SPEC: NL-CECC 90 104-040 ISSUED: 1984-11-01 In coherence with Family Specification NEN-CECC 90 104 ISSUE 1 1981		
DETAIL SPECIFICATION FOR HEF(HEC)4052B, dual 4-channel analogue multiplexer/demultiplexer TYPICAL CONSTRUCTION: LOCMOS, buffered (B) and unbuffered (UB) outputs, cavity and non-cavity packages. <i>CAUTION: STATIC SENSITIVE DEVICE</i>			
OUTLINES AND DIMENSIONS IEC 191-2-1-50a type C Dual in-line (plastic and ceramic). Leads are tin plated.	Assessment levels R, T and V		
1 TYPE DESCRIPTION 1.1 Function The HEF(HEC)4052B is a dual 4-channel analogue multiplexer/demultiplexer with common channel select logic. Each multiplexer/demultiplexer has four independent inputs/outputs (Y_0 to Y_3) and a common input/output (Z). The common channel select logic includes two address inputs (A_0 and A_1) and an active LOW enable input ($\bar{E}$). Both multiplexers/demultiplexers contain four bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 to Y_3) and the other side connected to a common input/output (Z). With $\bar{E}$ LOW, one of the four switches is selected (low impedance ON-state) by A_0 and A_1 . With $\bar{E}$ HIGH, all switches are in the high impedance OFF-state, independent of A_0 and A_1 . V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (A_0 , A_1 and $\bar{E}$). The V_{DD} to V_{SS} range is 3 to 15 V. The analogue inputs/outputs (Y_0 to Y_3 , and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD} - V_{EE}$ may not exceed 15 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).			
See the relevant Qualified Products List (QPL) for availability of components made to this specification.			



1.2.1 Logic diagram



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1.2.2 Schematic diagram

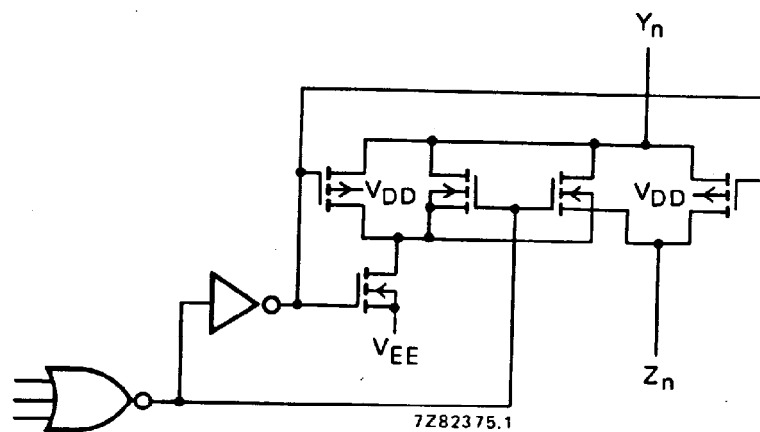


Fig. 3 Schematic diagram (one switch).

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1.3 Terminal identification, type designation, and marking

1.3.1 Terminal identification (top view)



Fig. 4 Pinning diagram.

1.3.2 Type designation

HEX4052BXX

HE	family identification
X	operating temperature range (C = full, F = limited)
4052	device number
B	JEDEC "B" series C-MOS specification
X	package code (P = plastic, D = ceramic)
X	B = burn-in (optional)

1.3.3 Marking

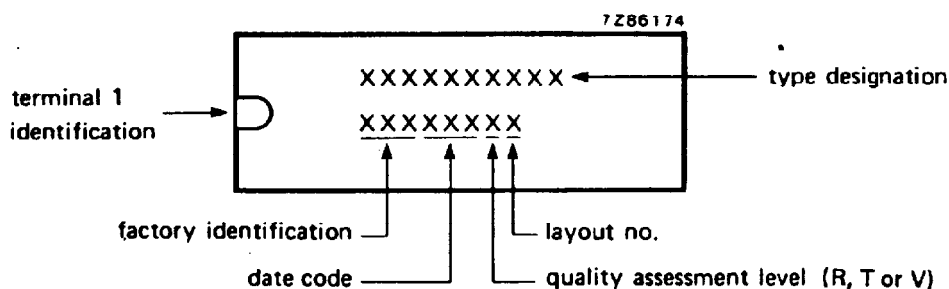


Fig. 5 Marking.

1.4 Ordering information

N (a) integrated circuits Philips HEF (b) 4052B, R (c) level, B class (d), D (e) package, following NL-CECC 90 104-040, Issue 1.

- a: Quantity.
- b: Operating temperature range (HEC or HEF).
- c: Quality assessment level (R, T or V).
- d: Burn-in (optional)
- e: Package code e.g. ceramic (P = plastic, D = ceramic).