

NEDERLANDS ELEKTROTECHNISCH
COMITE
POSTBOX 5059
2600 GB DELFT

This specification is also available from
Nederlandse Philips Bedrijven B.V.

CECC 90 104-040



ISSUE 3

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Total number of pages: 14

**ELECTRONIC COMPONENTS OF ASSESSED
QUALITY IN ACCORDANCE WITH:**

GS: CECC 90 000 Issue 3.
SS: CECC 90 100 Issue 3.
FS: CECC 90 104 Issue 2.

Detail Spec: NL-CECC 90 104-040

Issue: 3

Issued: December 1989

OUTLINE AND DIMENSIONS:

IEC 191-2 | 050 G09/A76 G1

TERMINAL CONNECTIONS:

See item 1.4 of this specification

DETAIL SPECIFICATION FOR
DIGITAL INTEGRATED CIRCUITS
IN ACCORDANCE WITH FS 90 104

HEC/HEF 4052B

Dual 4-channel analogue
multiplexer/demultiplexer

TYPICAL CONSTRUCTION:

Silicon monolithic local oxidation
CMOS integrated circuit, cavity/non-
cavity packages.

CAUTION: STATIC SENSITIVE DEVICE

ASSESSMENT LEVELS: P, Y, L

REMARKS

Supply voltage (with respect to V_{DD}) $V_{EE} = -18$ to $+0,5$ V.

Information about manufacturers who have components qualified to this detail specification is
available in the current CECC 00 200: Qualified Products List.



Documents

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1 TYPE DESCRIPTION

1.1 Function

The HEC/HEF4052B are dual 4-channel analogue multiplexers/demultiplexers with common channel select logic. Each multiplexer/demultiplexer has four independent inputs/outputs (Y_0 to Y_3) and a common input/output (Z). The common channel select logic includes two address inputs (A_0 and A_1) and an active LOW enable input ($\bar{E}$).

Both multiplexers/demultiplexers contain four bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 to Y_3) and the other side connected to a common input/output (Z).

With $\bar{E}$ LOW, one of the four switches is selected (low impedance ON-state) by A_0 and A_1 . With $\bar{E}$ HIGH, all switches are in the high impedance OFF-state, independent of A_0 and A_1 .

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (A_0 , A_1 and $\bar{E}$). The V_{DD} to V_{SS} range is 3 to 15 V. The analogue inputs/outputs (Y_0 to Y_3 , and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD} - V_{EE}$ may not exceed 15 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

1.1.1 Function table

inputs			channel ON
$\bar{E}$	A_1	A_0	
L	L	L	$Y_{0A}-Z_A; Y_{0B}-Z_B$
L	L	H	$Y_{1A}-Z_A; Y_{1B}-Z_B$
L	H	L	$Y_{2A}-Z_A; Y_{2B}-Z_B$
L	H	H	$Y_{3A}-Z_A; Y_{3B}-Z_B$
H	X	X	none

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial



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1.1.2 Functional diagram

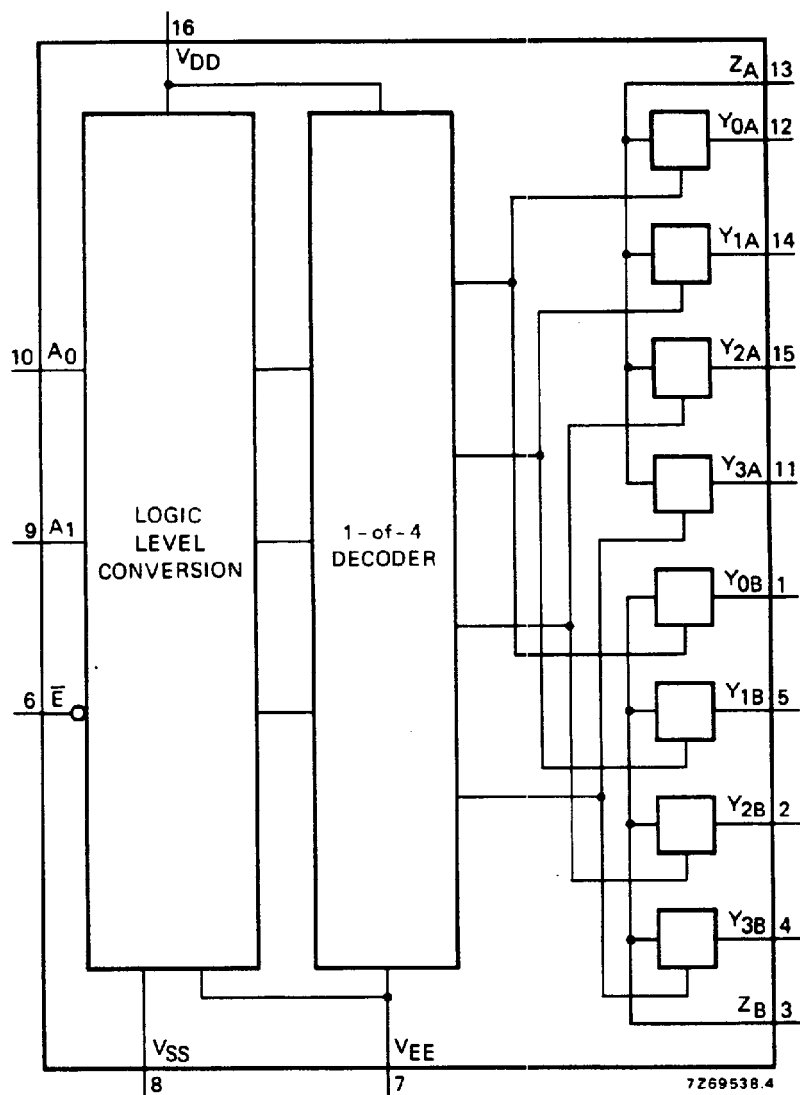


Fig. 1 Functional diagram.

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1.1.3 Pinning information

Y_{0A} to Y_{3A} independent inputs/outputs
 Y_{0B} to Y_{3B} independent inputs/outputs
 A₀, A₁ address inputs
 $\bar{E}$ enable input (active LOW)
 Z_A, Z_B common inputs/outputs

1.2 Schematic diagram

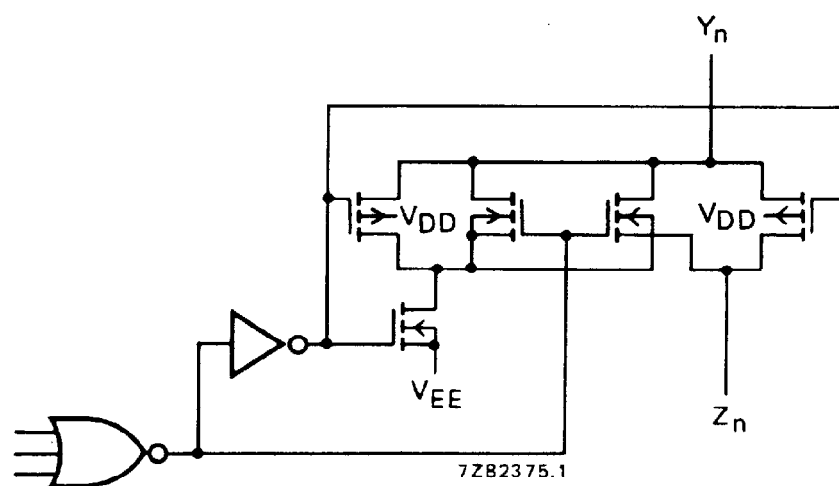


Fig. 2 Schematic diagram (one switch).

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1.3 Logic diagram

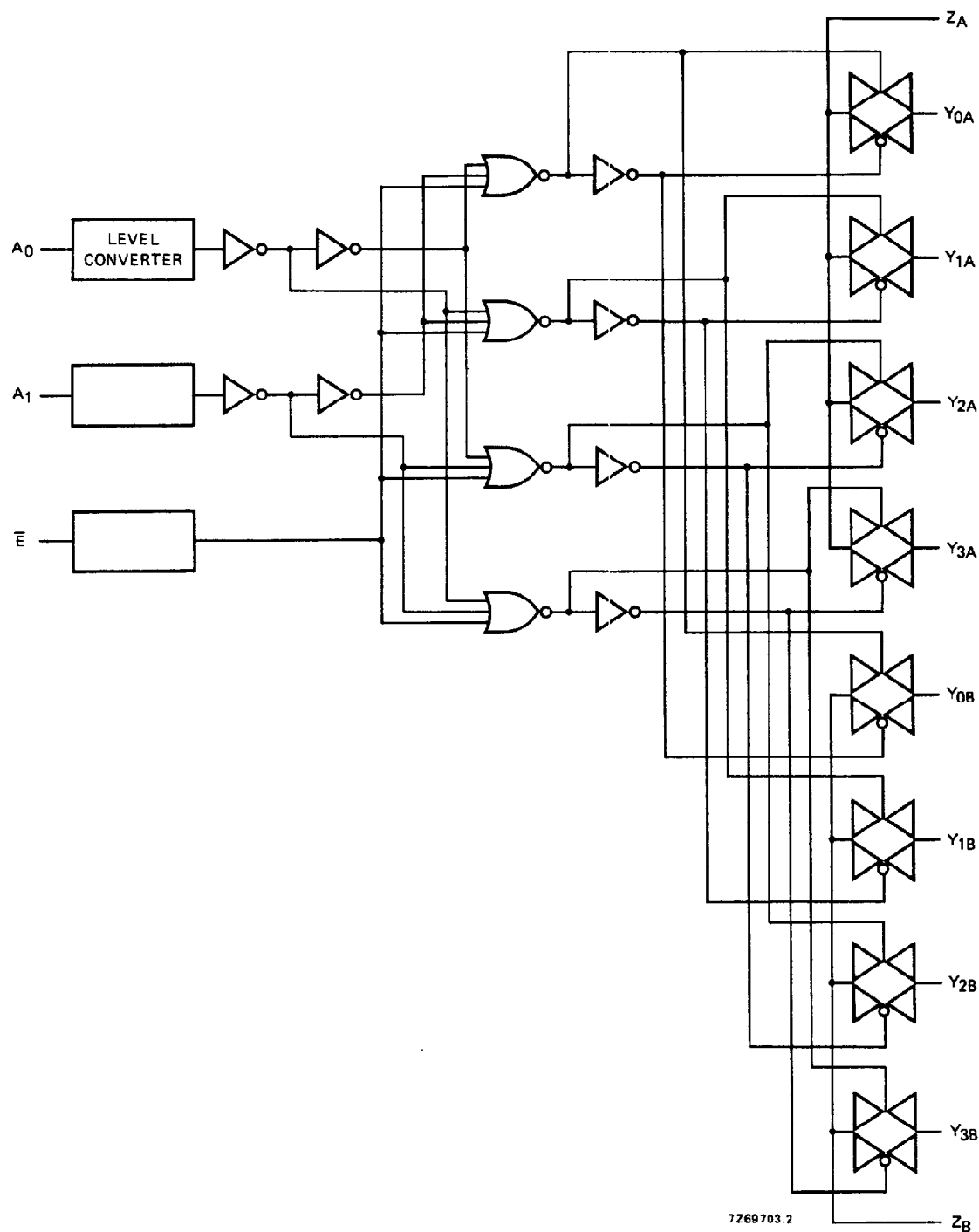


Fig. 3 Logic diagram.