

NEDERLANDS ELEKTROTECHNISCH  
COMITE  
POSTBOX 5059  
2600 GB DELFT

This specification is also available from  
Nederlandse Philips Bedrijven B.V.

CECC 90 104-065



ISSUE 2

Page 1

Total number of pages: 16

**ELECTRONIC COMPONENTS OF ASSESSED  
QUALITY IN ACCORDANCE WITH:**

GS: CECC 90 000 Issue 3.  
SS: CECC 90 100 Issue 3.  
FS: CECC 90 104 Issue 2.

Detail Spec: NL—CECC 90 104-065

Issue: 2

Issued: December 1989

**OUTLINE AND DIMENSIONS:**

IEC 191-2 | 050 G09/A76 G1

**TERMINAL CONNECTIONS:**

See item 1.4 of this specification

**DETAIL SPECIFICATION FOR  
DIGITAL INTEGRATED CIRCUITS  
IN ACCORDANCE WITH FS 90 104**

**HEC/HEF4511B**

BCD to 7-segment latch/decoder/driver

**TYPICAL CONSTRUCTION:**

Silicon monolithic local oxidation  
CMOS integrated circuit, cavity/non-  
cavity packages.

**CAUTION: STATIC SENSITIVE DEVICE**

**ASSESSMENT LEVELS: P, Y, L**

**REMARKS**

Information about manufacturers who have components qualified to this detail specification is  
available in the current CECC 00 200: Qualified Products List.



**Documents**

Document Sharing Hub

|                                                                                                                                                            |                             |                                        |
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## 1 TYPE DESCRIPTION

### 1.1 Function

The HEC/HEF4511B are BCD to 7-segment latches/decoders/drivers with four address inputs ( $D_A$  to  $D_D$ ) an active LOW latch enable input ( $\overline{EL}$ ), an active LOW ripple blanking input ( $\overline{BI}$ ), an active LOW lamp test input ( $\overline{LT}$ ), and seven active HIGH n-p-n bipolar transistor segment outputs ( $O_a$  to  $O_g$ ).

When  $\overline{EL}$  is LOW, the state of the segment outputs ( $O_a$  to  $O_g$ ) is determined by the data on  $D_A$  to  $D_D$ . When  $\overline{EL}$  goes HIGH, the last data present on  $D_A$  to  $D_D$  are stored in the latches and the segment outputs remain stable. When  $\overline{LT}$  is LOW, all the segment outputs are HIGH independent of all other input conditions. With  $\overline{LT}$  HIGH, a LOW on  $\overline{BI}$  forces all segment outputs LOW. The inputs  $\overline{LT}$  and  $\overline{BI}$  do not affect the latch circuit.

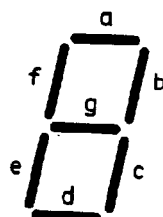


Fig. 1 Segment designation.

|                                                                                 |        |                 |
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## 1.1.1 Function table

| inputs          |                 |                 |                |                |                |                | outputs        |                |                |                |                |                |                |         |
|-----------------|-----------------|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|---------|
| $\overline{EL}$ | $\overline{BI}$ | $\overline{LT}$ | D <sub>D</sub> | D <sub>C</sub> | D <sub>B</sub> | D <sub>A</sub> | O <sub>a</sub> | O <sub>b</sub> | O <sub>c</sub> | O <sub>d</sub> | O <sub>e</sub> | O <sub>f</sub> | O <sub>g</sub> | display |
| X               | X               | L               | X              | X              | X              | X              | H              | H              | H              | H              | H              | H              | H              | 8       |
| X               | L               | H               | X              | X              | X              | X              | L              | L              | L              | L              | L              | L              | L              | blank   |
| L               | H               | H               | L              | L              | L              | L              | H              | H              | H              | H              | H              | H              | L              | 0       |
| L               | H               | H               | L              | L              | L              | H              | L              | H              | H              | L              | L              | L              | L              | 1       |
| L               | H               | H               | L              | L              | H              | L              | H              | H              | L              | H              | L              | L              | H              | 2       |
| L               | H               | H               | L              | L              | H              | H              | H              | H              | H              | H              | L              | L              | H              | 3       |
| L               | H               | H               | L              | H              | L              | L              | L              | H              | H              | L              | L              | H              | H              | 4       |
| L               | H               | H               | L              | H              | L              | H              | H              | L              | H              | H              | L              | H              | H              | 5       |
| L               | H               | H               | L              | H              | H              | L              | L              | L              | H              | H              | H              | H              | H              | 6       |
| L               | H               | H               | L              | H              | H              | H              | H              | H              | H              | L              | L              | L              | L              | 7       |
| L               | H               | H               | H              | L              | L              | L              | H              | H              | H              | H              | H              | H              | H              | 8       |
| L               | H               | H               | H              | L              | L              | H              | H              | H              | H              | L              | L              | H              | H              | 9       |
| L               | H               | H               | H              | L              | H              | L              | L              | L              | L              | L              | L              | L              | L              | blank   |
| L               | H               | H               | H              | L              | H              | H              | L              | L              | L              | L              | L              | L              | L              | blank   |
| L               | H               | H               | H              | H              | L              | L              | L              | L              | L              | L              | L              | L              | L              | blank   |
| L               | H               | H               | H              | H              | L              | H              | L              | L              | L              | L              | L              | L              | L              | blank   |
| L               | H               | H               | H              | H              | H              | L              | L              | L              | L              | L              | L              | L              | L              | blank   |
| H               | H               | H               | X              | X              | X              | X              |                |                |                | *              |                |                |                | *       |

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

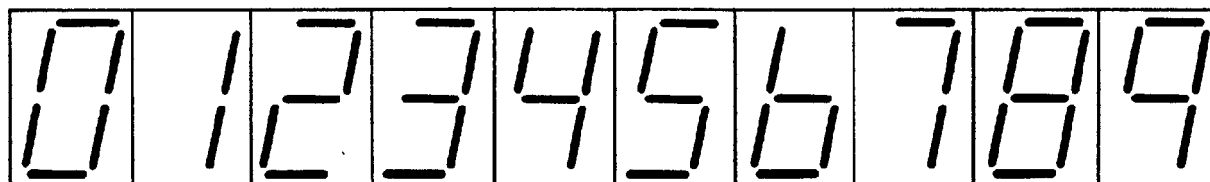
\* Depends upon the BCD code applied during the LOW to HIGH transition of  $\overline{EL}$ .

Fig. 2 Display.

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|                                                                                 |        |                 |
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### 1.1.2 Functional diagram

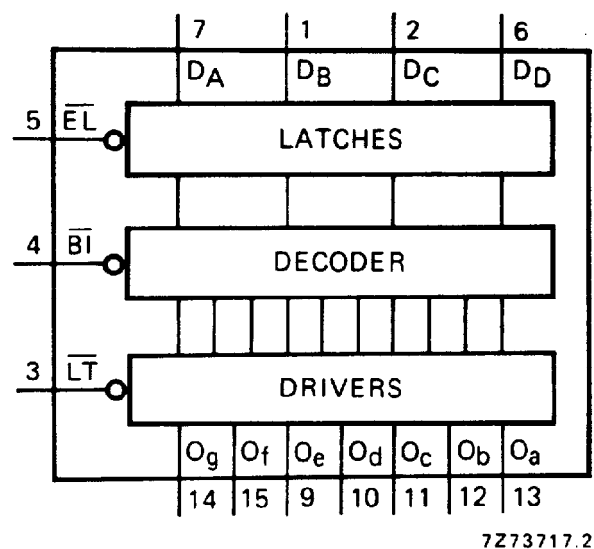


Fig. 3 Functional diagram.

### 1.1.3 Pinning information

|                 |                                    |
|-----------------|------------------------------------|
| $D_A$ to $D_D$  | address (data) inputs              |
| $\overline{EL}$ | latch enable input (active LOW)    |
| $\overline{BI}$ | ripple blanking input (active LOW) |
| $\overline{LT}$ | lamp test input (active LOW)       |
| $O_a$ to $O_g$  | segment outputs                    |

|                                                                                                                                                                      |                            |                                       |
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## 1.2 Schematic diagram

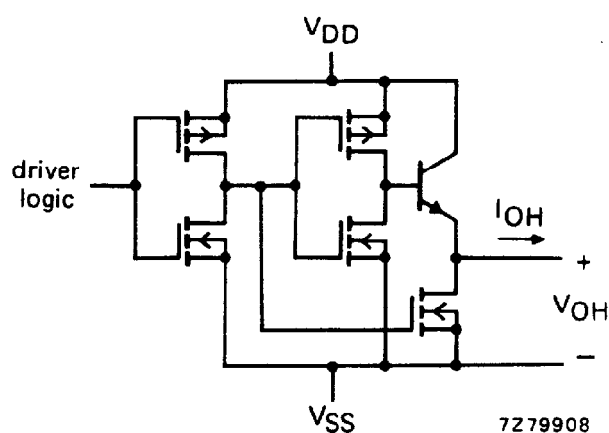


Fig. 4 Schematic diagram of output stage.

## 1.3 Logic diagram

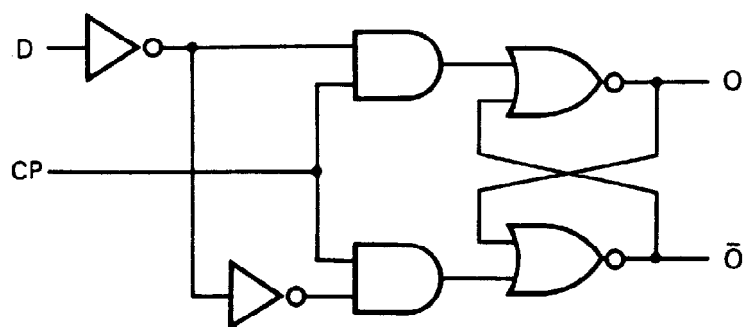


Fig. 5 Logic diagram (one latch); see also Fig. 6.