

NEDERLANDS ELEKTROTECHNISCH
COMITE
POSTBOX 5059
2600 GB DELFT

This specification is also available from
Nederlandse Philips Bedrijven B.V.

CECC 90 104-074



ISSUE 2

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ELECTRONIC COMPONENTS OF ASSESSED QUALITY IN ACCORDANCE WITH:

GS: CECC 90 000 Issue 3.
SS: CECC 90 100 Issue 3.
FS: CECC 90 104 Issue 2.

Detail Spec: NL—CECC 90 104-074

Issue: 2

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OUTLINE AND DIMENSIONS:

IEC 191-2 | 050 G09/A76 G1

TERMINAL CONNECTIONS:

See item 1.4 of this specification

DETAIL SPECIFICATION FOR DIGITAL INTEGRATED CIRCUITS IN ACCORDANCE WITH FS 90 104

HEC/HEF 4521B

24-stage frequency divider

TYPICAL CONSTRUCTION:

Silicon monolithic local oxidation
CMOS integrated circuit, cavity/non-
cavity packages.

CAUTION: STATIC SENSITIVE DEVICE

ASSESSMENT LEVELS: P, Y, L

REMARKS

Information about manufacturers who have components qualified to this detail specification is
available in the current CECC 00 200: Qualified Products List.



Documents

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1 TYPE DESCRIPTION

1.1 Function

The HEC/HEF4521B each consist of a chain of 24 toggle flip-flops with an overriding asynchronous master reset input (MR), and an input circuit that allows three modes of operation. The single inverting stage (I_2/O_2) will function as a crystal oscillator, or in combination with I_1 as an RC oscillator, or as an input buffer for an external oscillator. Low-power operation as a crystal oscillator is enabled by connecting external resistors to pins 3 (V_{SS}') and 5 (V_{DD}').

Each flip-flop divides the frequency of the previous flip-flop by two, consequently the HEC/HEF4521B will count up to $2^{24} = 16\,777\,216$. The counting advances on the HIGH to LOW transition of the clock (I_2). The outputs of the last seven stages are available for additional flexibility.

1.1.1 Count capacity

output	count capacity
O ₁₈	$2^{18} = 262\,144$
O ₁₉	$2^{19} = 524\,288$
O ₂₀	$2^{20} = 1\,048\,576$
O ₂₁	$2^{21} = 2\,097\,152$
O ₂₂	$2^{22} = 4\,194\,304$
O ₂₃	$2^{23} = 8\,388\,608$
O ₂₄	$2^{24} = 16\,777\,216$

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1.1.2 Functional test sequence

inputs		control terminals			outputs	remarks
MR	I ₂	O ₂	V _{SS} '	V _{DD} '	O ₁₈ to O ₂₄	
H	L	L	V _{DD}	V _{SS}	L	counter is in three 8-stage sections in parallel mode; I ₂ and O ₂ are interconnected (O ₂ is now input); counter is reset by MR
L			V _{DD}	V _{SS}	H	255 pulses are clocked into I ₂ , O ₂ (the counter advances on the LOW to HIGH transition)
L	L	L	V _{SS}	V _{SS}	H	V _{SS} ' is connected to V _{SS}
L	H	L	V _{SS}	V _{SS}	H	the input I ₂ is made HIGH
L	H	L	V _{SS}	V _{DD}	H	V _{DD} ' is connected to V _{DD} ; O ₂ is now made floating and becomes an output; the device is now in the 2 ²⁴ mode
L			V _{SS}	V _{DD}	L	counter ripples from an all HIGH state to an all LOW state

A test function has been included for the reduction of the test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections by connecting V_{SS}' to V_{DD} and V_{DD}' to V_{SS}. Via I₂ (connected to O₂) 255 counts are loaded into each of the 8-stage sections in parallel. All flip-flops are now at a HIGH state. The counter is now returned to the normal 24-stage in series configuration by connecting V_{SS}' to V_{SS} and V_{DD}' to V_{DD}. One more pulse is entered into input I₂, which will cause the counter to ripple from an all HIGH state to an all LOW state.

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1.1.4 Pinning information

1.2 Schematic diagram

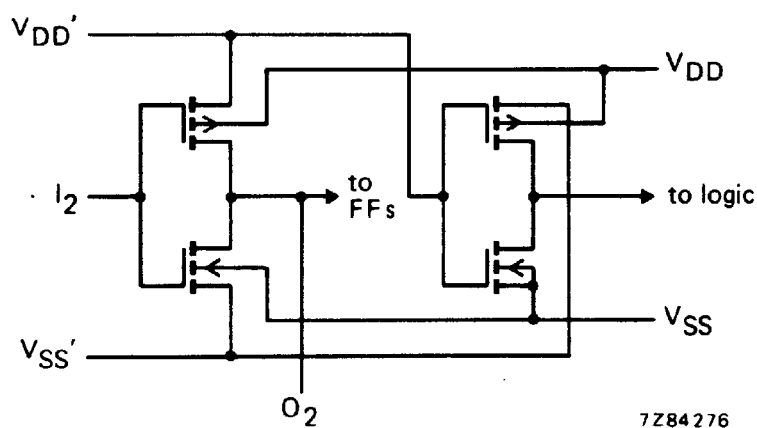


Fig. 2 Schematic diagram of clock input circuitry.