

NEDERLANDS ELEKTROTECHNISCH
COMITE
POSTBOX 5059
2600 GB DELFT

This specification is also available from
Nederlandse Philips Bedrijven B.V.

CECC 90 104-094



ISSUE 2

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**ELECTRONIC COMPONENTS OF ASSESSED
QUALITY IN ACCORDANCE WITH:**

GS: CECC 90 000 Issue 3.
SS: CECC 90 100 Issue 3.
FS: CECC 90 104 Issue 2.

Detail Spec: NL-CECC 90 104-094

Issue: 2

Issued: December 1989

OUTLINE AND DIMENSIONS:

IEC 191-2 | 050 G09/A76 G1

TERMINAL CONNECTIONS:

See item 1.3 of this specification

**DETAIL SPECIFICATION FOR
DIGITAL INTEGRATED CIRCUITS
IN ACCORDANCE WITH FS 90 104**

HEC/HEF40161B

4-bit synchronous binary counter
with asynchronous reset

TYPICAL CONSTRUCTION:

Silicon monolithic local oxidation
CMOS integrated circuit, cavity/non-
cavity packages.

CAUTION: STATIC SENSITIVE DEVICE

ASSESSMENT LEVELS: P, Y, L

REMARKS

Information about manufacturers who have components qualified to this detail specification is
available in the current CECC 00 200: Qualified Products List.



Documents

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1 TYPE DESCRIPTION

1.1 Function

The HEC/HEF40161B are fully synchronous edge-triggered 4-bit binary counters with a clock input (CP), an overriding asynchronous master reset ($\overline{MR}$), four parallel data inputs (P_0 to P_3), three synchronous mode control inputs (parallel enable ($\overline{PE}$), count enable parallel (CEP) and count enable trickle (CET)), buffered outputs from all four bit positions (O_0 to O_3) and a terminal count output (TC).

Operation is fully synchronous (except for the $\overline{MR}$ input) and occurs on the LOW to HIGH transition of CP. When $\overline{PE}$ is LOW, the next LOW to HIGH transition of CP loads data into the counter from P_0 to P_3 regardless of the levels of CEP and CET inputs.

When $\overline{PE}$ is HIGH, the next LOW to HIGH transition of CP advances the counter to its next state only if both CEP and CET are HIGH; otherwise, no change occurs in the state of the counter. TC is HIGH when the state of the counter is 15 (O_1 to O_3 = HIGH) and when CET is HIGH. A LOW on $\overline{MR}$ sets all outputs (O_0 to O_3 and TC) LOW, independent of the state of all other inputs. Multistage synchronous counting is possible without additional components by using a carry look-ahead counting technique; in this case, TC is used to enable successive cascaded stages. CEP, CET and $\overline{PE}$ must be stable only during the set-up time before the LOW to HIGH transition of CP.

1.1.1 Synchronous mode selection table

$\overline{PE}$	CEP	CET	mode
L	X	X	preset
H	L	X	no change
H	X	L	no change
H	H	H	count

$\overline{MR}$ = HIGH

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

1.1.2 Terminal count generation table

CET	($O_0 \cdot O_1 \cdot O_2 \cdot O_3$)	TC
L	L	L
L	H	L
H	L	L
H	H	H

$$TC = CET \cdot O_0 \cdot O_1 \cdot O_2 \cdot O_3$$

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1.1.3 State diagram

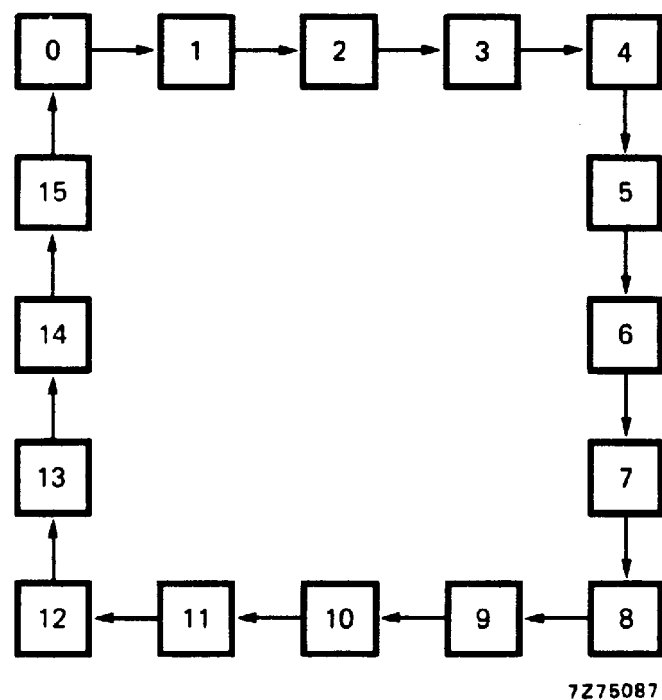


Fig. 1 State diagram.

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1.1.4 Functional diagram

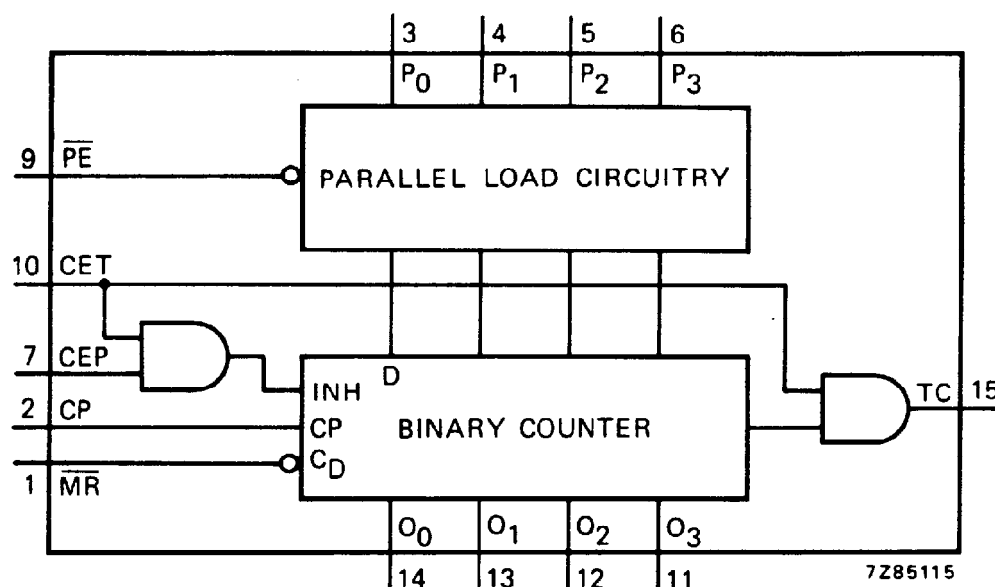


Fig. 2 Functional diagram.

1.1.5 Pinning information

$\overline{PE}$	parallel enable input
P_0 to P_3	parallel data inputs
CEP	count enable parallel input
CET	count enable trickle input
CP	clock input (LOW to HIGH, edge-triggered)
$\overline{MR}$	master reset input (active LOW)
O_0 to O_3	parallel outputs
TC	terminal count output

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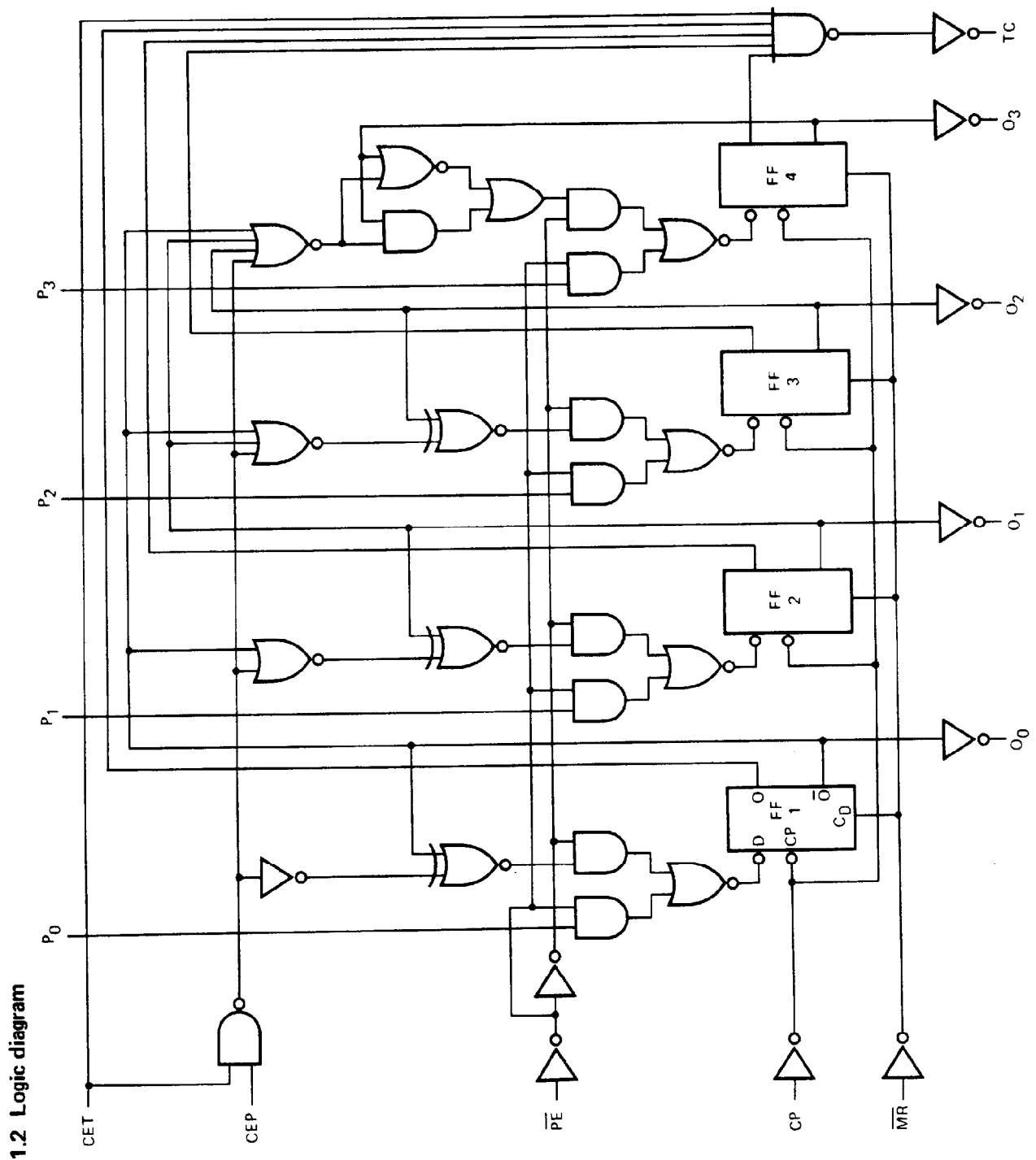


Fig. 3 Logic diagram.