

1. Limiting conditions of use (contd)

1.5	Maximum power dissipation, per package	P_{D1}	200,0mW
	per output	P_{D2}	50,0mW
1.6	Maximum continuous current into any input.	$ I_I $	10,0mA
1.7	Maximum continuous current into any output.	$ I_O $	10,0mA
1.8	Operating temperature range	T_{amb}	
		Full	-55 to +125°C
		Limited	-40 to + 85°C
1.9	Storage temperature range	T_{stg}	-65 to +150°C
1.10	Transient energy rating		400V at 100pF through 1,5kΩ
1.11	<u>Recommended handling precautions</u>		
1.11.1	Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method.		
1.11.2	Use grounded tip soldering irons.		
1.11.3	Ground all test equipment.		
1.11.4	Connect all unused device inputs to V_{DD} or V_{SS} .		
1.11.5	PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations.		
1.11.6	Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices.		
1.11.7	Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during inspection or handling.		
1.11.8	When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage, 'Dummy connectors' should be used to electrically short all PC board terminals together.		
1.11.9	Switch off power supply before inserting or removing devices from circuits.		
1.11.10	Disconnect all low impedance equipment and input signals from the device before d.c. power supplies are switched off.		

2. Recommended conditions of use and associated characteristics (not for inspection purposes)

These apply over the operating temperature range unless otherwise stated. All voltages referenced to V_{SS} .

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Quiescent device current	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range	Outputs open circuit	I_{DDA}	5,0	5,0	5,0	150,0	μA
		I_{DDA}	10,0	10,0	10,0	300,0	μA
		I_{DDA}	15,0	20,0	20,0	600,0	μA
Limited temperature range		I_{DDA}	5,0	20,0	20,0	150,0	μA
		I_{DDA}	10,0	40,0	40,0	300,0	μA
		I_{DDA}	15,0	80,0	80,0	600,0	μA
LOW level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OLA}	5,0	0,05	0,05	0,05	V
		V_{OLA}	10,0	0,05	0,05	0,05	V
		V_{OLA}	15,0	0,05	0,05	0,05	V
HIGH level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OHB}	5,0	4,95	4,95	4,95	V
		V_{OHB}	10,0	9,95	9,95	9,95	V
		V_{OHB}	15,0	14,95	14,95	14,95	V
LOW level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IL} = 1,5V$ $V_{IL} = 3,0V$ $V_{IL} = 4,0V$	V_{OLA}	5,0	0,5	0,5	0,5	V
		V_{OLA}	10,0	1,0	1,0	1,0	V
		V_{OLA}	15,0	1,5	1,5	1,5	V
HIGH level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IH} = 3,5V$ $V_{IH} = 7,0V$ $V_{IH} = 11,0V$	V_{OHB}	5,0	4,5	4,5	4,5	V
		V_{OHB}	10,0	9,0	9,0	9,0	V
		V_{OHB}	15,0	13,5	13,5	13,5	V
Output LOW (sink) current							
Full temperature range	$V_O = 0,4V$ $V_O = 0,5V$ $V_O = 1,5V$	I_{OLB}	5,0	0,64	0,51	0,36	mA
		I_{OLB}	10,0	1,60	1,30	0,90	mA
		I_{OLB}	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_O = 0,4V$ $V_O = 0,5V$ $V_O = 1,5V$	I_{OLB}	5,0	0,52	0,44	0,36	mA
		I_{OLB}	10,0	1,30	1,10	0,90	mA
		I_{OLB}	15,0	3,60	3,00	2,40	mA

Characteristics	Conditions	Symbol	V_{DD} (V)	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Output HIGH (source) current							
Full temperature range	$V_O = 4,6V$	$-I_{OHB}$	5,0	0,64	0,51	0,36	mA
	$V_O = 9,5V$	$-I_{OHB}$	10,0	1,60	1,30	0,90	mA
	$V_O = 13,5V$	$-I_{OHB}$	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_O = 4,6V$	$-I_{OHB}$	5,0	0,52	0,44	0,36	mA
	$V_O = 9,5V$	$-I_{OHB}$	10,0	1,30	1,10	0,90	mA
	$V_O = 13,5V$	$-I_{OHB}$	15,0	3,60	3,00	2,40	mA
Input leakage current	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range		$ I_{IA} $	15,0	0,10	0,10	1,00	μA
Limited temperature range		$ I_{IA} $	15,0	0,30	0,30	1,00	μA
Three state output leakage current (combined to obtain a high impedance output state)	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range		$ I_{OZA} $	15,0	0,4	0,4	12,0	μA
Limited temperature range		$ I_{OZA} $	15,0	1,6	1,6	12,0	μA
Input capacitance per unit load (Any input)	$V_I = 0V$ $f = 1MHz$	C_{IA}	-	-	7,5	-	pF
Noise margin at LOW level output (equal to the difference between V_{IL} and V_{OL} for worst case combinations)		V_{NLB}	5,0	1,0	1,0	1,0	V
		V_{NLB}	10,0	2,0	2,0	2,0	V
		V_{NLB}	15,0	2,5	2,5	2,5	V
Noise margin at HIGH level output (equal to the difference between V_{IH} and V_{OH} for worst case combinations)		V_{NHB}	5,0	1,0	1,0	1,0	V
		V_{NHB}	10,0	2,0	2,0	2,0	V
		V_{NHB}	15,0	2,5	2,5	2,5	V

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25°C	T _{amb} HIGH	Unit
Propagation and Transition Times	C _L = 50pF (Test conditions as in Sub-group A5)						
Transition Time LOW to HIGH level		t _{TLHA}	5,0	-	360,0	-	ns
		t _{TLHA}	10,0	-	180,0	-	ns
		t _{TLHA}	15,0	-	130,0	-	ns
Transition Time HIGH to LOW level		t _{THLA}	5,0	-	200,0	-	ns
		t _{THLA}	10,0	-	100,0	-	ns
		t _{THLA}	15,0	-	80,0	-	ns
Propagation Delay Time HIGH to LOW and LOW to HIGH level Clock to Q Reset to Q		t _{PLHA} /	5,0	-	600,0	-	ns
		t _{PHLA}	10,0	-	250,0	-	ns
			15,0	-	180,0	-	ns
Clock Pulse Width		t _{PWCB}	5,0	-	260,0	-	ns
		t _{PWCB}	10,0	-	110,0	-	ns
		t _{PWCB}	15,0	-	80,0	-	ns
Clock Pulse Frequency		Freq A	5,0	-	1,80	-	MHz
		Freq A	10,0	-	4,50	-	MHz
		Freq A	15,0	-	6,00	-	MHz
Clock Rise and Fall Times		t _{rA} , t _{fA}	5,0	-	15,0	-	μs
		t _{rA} , t _{fA}	10,0	-	15,0	-	μs
		t _{rA} , t _{fA}	15,0	-	15,0	-	μs
Reset Pulse Width		t _{PWRB}	5,0	-	370,0	-	ns
		t _{PWRB}	10,0	-	150,0	-	ns
		t _{PWRB}	15,0	-	110,0	-	ns
Data Set-up Time		t _{PWSTA}	5,0	-	200,0	-	ns
		t _{PWSTA}	10,0	-	80,0	-	ns
		t _{PWSTA}	15,0	-	60,0	-	ns
Data Hold Time		t _{PWHA}	5,0	-	130,0	-	ns
		t _{PWHA}	10,0	-	60,0	-	ns
		t _{PWHA}	15,0	-	50,0	-	ns

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25°C	T _{amb} HIGH	Unit
Data Disable Set-up Time		t _{PWSTA}	5,0	-	220,0	-	ns
		t _{PWSTA}	10,0	-	80,0	-	ns
		t _{PWSTA}	15,0	-	50,0	-	ns
HIGH or LOW level to High impedance Propagation Delay Time		t _{PHZA} /	5,0	-	300,0	-	ns
		t _{PLZA}	10,0	-	140,0	-	ns
		t _{PLZA}	15,0	-	115,0	-	ns
High impedance to HIGH or LOW level		t _{PZHA} /	5,0	-	400,0	-	ns
		t _{PZLA}	10,0	-	160,0	-	ns
		t _{PZLA}	15,0	-	120,0	-	ns

Terminal identification

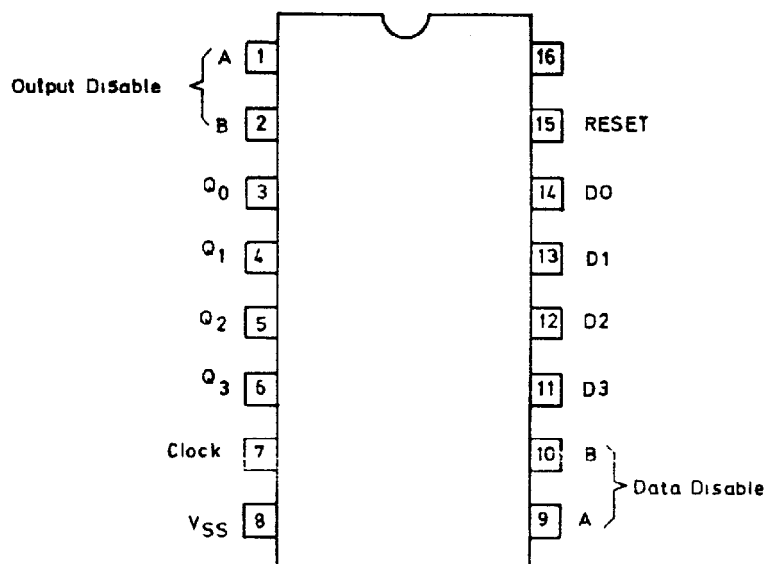


Figure 1

Function table

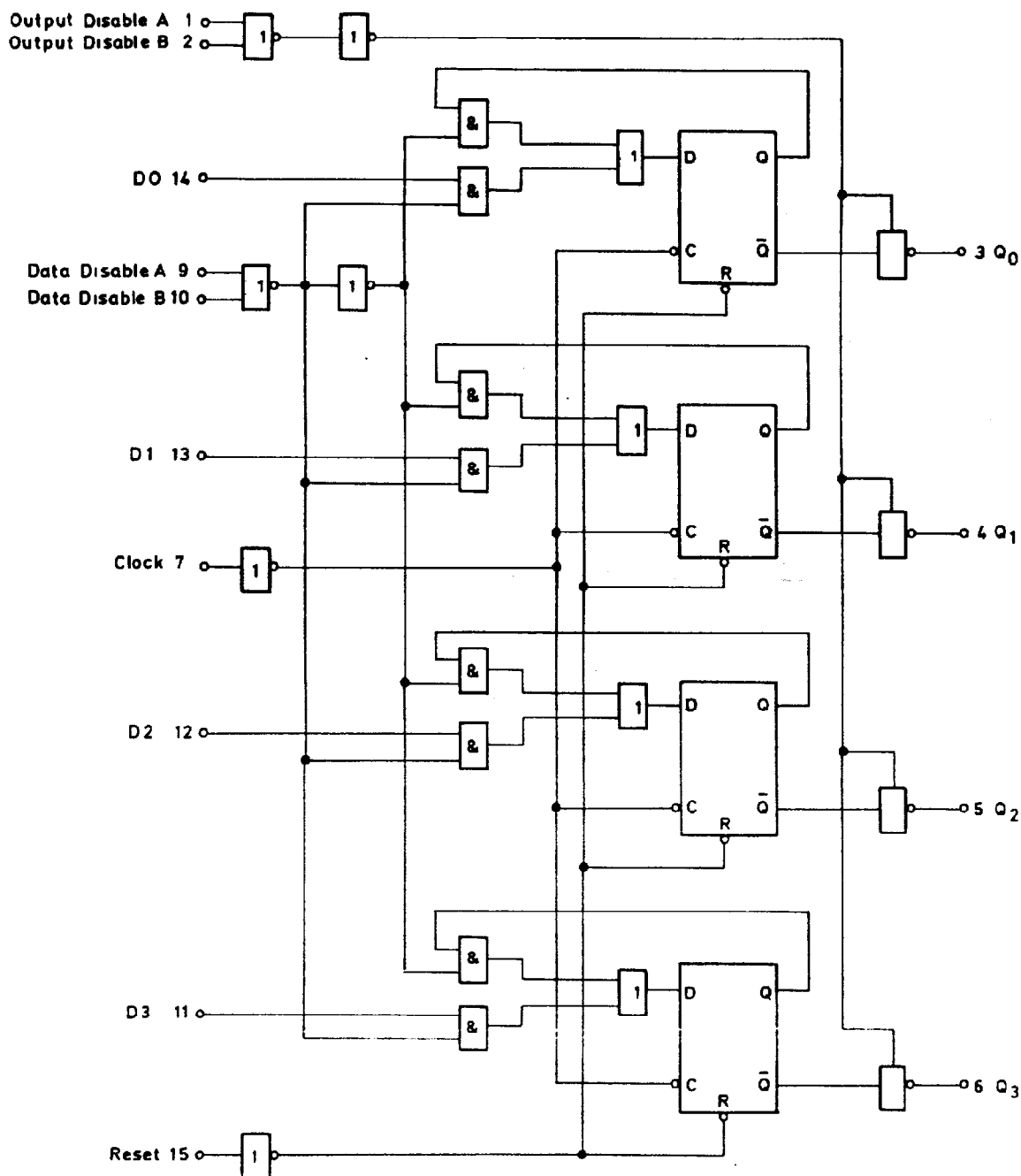
Table 1

INPUTS					OUTPUT Q
RESET	CLOCK	DATA DISABLE		DATA D	
		A	B		
H	X	X	X	X	L
L	L	X	X	X	Q_n
L		H	X	X	Q_n
L		X	H	X	Q_n
L		L	L	L	L
L		L	L	H	H

When either output disable A or B (or both) is (are) HIGH the output is disabled to the high impedance state; however sequential operation of the bistable is not affected.

H = HIGH level
L = LOW level
X = Level irrelevant

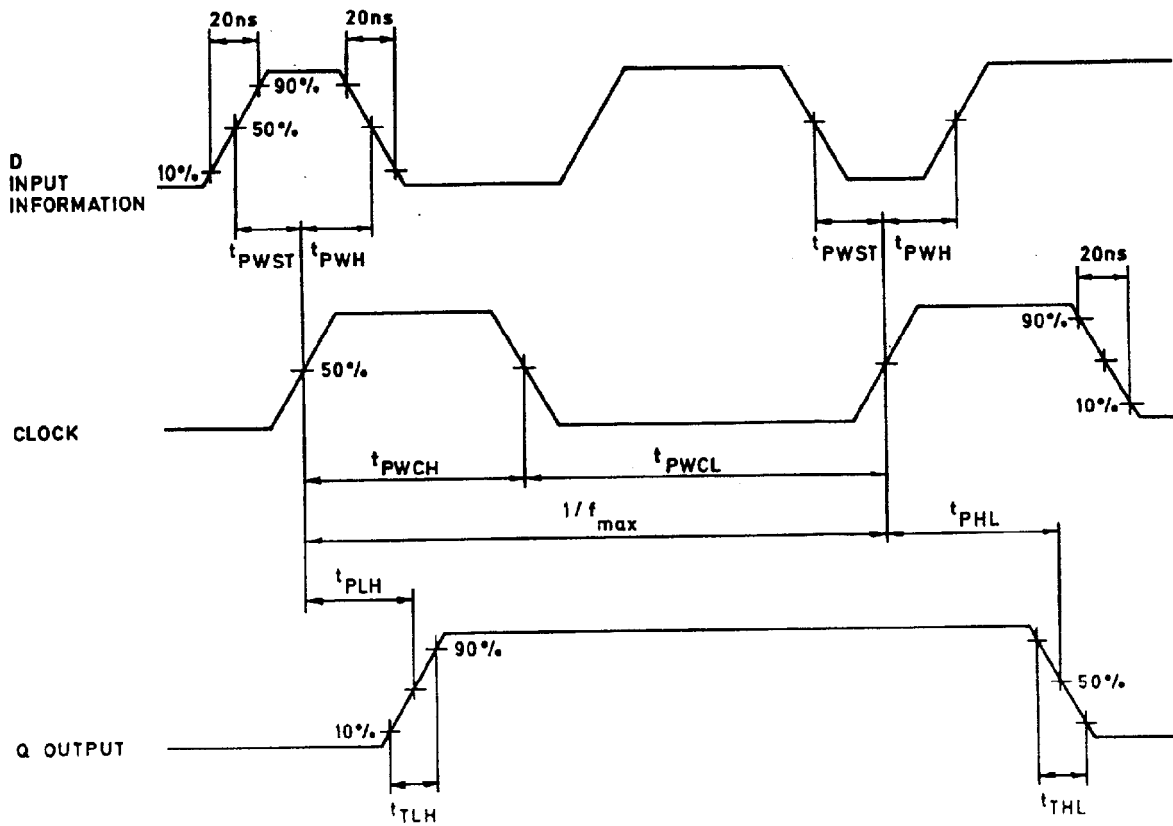
Typical logic diagram



This is a graphic representation, not a circuit diagram.

Figure 2

Switching time waveforms



Reset = L
Data Disable A and B = L
Output Disable A and B = L

Figure 3