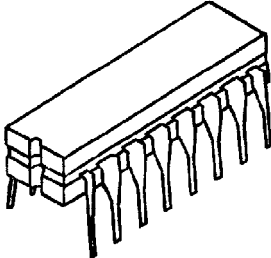


|                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                 |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>BRITISH STANDARDS INSTITUTION</b><br>2 PARK STREET, LONDON. W1A 2BS                                                                                                                                                    | BS CECC 90 104 - 150<br><br>ISSUE 1<br><br>DECEMBER 1981<br><br>Page 1 of 26 pages                                                                                                                                                              |
| Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND                                                                                                                                                    | <br><br><b>4099B</b><br>SEE PD 9002 AND CECC 00 200<br>For ordering information see page 11                                                                  |
| ELECTRONIC COMPONENTS OF ASSESSED QUALITY<br>DETAIL SPECIFICATION IN ACCORDANCE WITH:<br><br>BS CECC 90 000 : 1976<br>BS CECC 90 100 : 1977                                                                               | MANUFACTURERS TYPE NUMBER<br><br><b>4099B</b><br>SEE PD 9002 AND CECC 00 200<br>For ordering information see page 11                                                                                                                            |
| Outline not to scale: Isometric projection<br>Marking information see page 10<br><br><br><br>For detail dimensions see IEC 191-2 (A50C) | 8 BIT ADDRESSABLE LATCH<br>SERIAL INPUT/PARALLEL OUTPUT<br><br>SILICON COMPLEMENTARY MOS.<br>WITH (B) BUFFERED OUTPUTS AND<br>CAVITY PACKAGING.<br><br>Assessment levels<br>R, S, T and V<br>and optional screening<br>categories A, B, C and D |

CAUTION: THESE ARE STATIC SENSITIVE DEVICES - See clause 1.11

1. Limiting conditions of use (not for inspection purposes)

All voltages referenced to  $V_{SS}$

|     |                                  |          |                |
|-----|----------------------------------|----------|----------------|
| 1.1 | Maximum supply voltage, positive | $V_{DD}$ | +18,0V         |
| 1.2 | Maximum supply voltage, negative | $V_{DD}$ | -0,5V          |
| 1.3 | Maximum positive input voltage   | $V_I$    | $V_{DD}$ +0,5V |
| 1.4 | Maximum negative input voltage   | $V_I$    | -0,5V          |

Refer to Qualified Products List PD 9002 and/or CECC 00 200 for details of manufacturers approved to this specification

1. Limiting conditions of use (contd)

|         |                                                                                                                                                                                                  |           |                                |
|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|--------------------------------|
| 1.5     | Maximum power dissipation, per package                                                                                                                                                           | $P_{D1}$  | 200,0mW                        |
|         | per output                                                                                                                                                                                       | $P_{D2}$  | 25,0mW                         |
| 1.6     | Maximum continuous current into any input.                                                                                                                                                       | $ I_I $   | 10,0mA                         |
| 1.7     | Maximum continuous current into any output.                                                                                                                                                      | $ I_O $   | 10,0mA                         |
| 1.8     | Operating temperature range                                                                                                                                                                      | $T_{amb}$ |                                |
|         |                                                                                                                                                                                                  | Full      | -55 to +125°C                  |
|         |                                                                                                                                                                                                  | Limited   | -40 to + 85°C                  |
| 1.9     | Storage temperature range                                                                                                                                                                        | $T_{stg}$ | -65 to +150°C                  |
| 1.10    | Transient energy rating                                                                                                                                                                          |           | 400V at 100pF<br>through 1,5kΩ |
| 1.11    | <u>Recommended handling precautions</u>                                                                                                                                                          |           |                                |
| 1.11.1  | Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method.                                                           |           |                                |
| 1.11.2  | Use grounded tip soldering irons.                                                                                                                                                                |           |                                |
| 1.11.3  | Ground all test equipment.                                                                                                                                                                       |           |                                |
| 1.11.4  | Connect all unused device inputs to $V_{DD}$ or $V_{SS}$ .                                                                                                                                       |           |                                |
| 1.11.5  | PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations.                                                                    |           |                                |
| 1.11.6  | Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices.                                                           |           |                                |
| 1.11.7  | Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during inspection or handling.               |           |                                |
| 1.11.8  | When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage, 'Dummy connectors' should be used to electrically short all PC board terminals together. |           |                                |
| 1.11.9  | Switch off power supply before inserting or removing devices from circuits.                                                                                                                      |           |                                |
| 1.11.10 | Disconnect all low impedance equipment and input signals from the device before d.c. power supplies are switched off.                                                                            |           |                                |

2. Recommended conditions of use and associated characteristics (not for inspection purposes)

These apply over the operating temperature range unless otherwise stated. All voltages referenced to  $V_{SS}$ .

| Characteristics                                                               | Conditions                                             | Symbol    | $V_{DD}(V)$ | $T_{amb}$<br>LOW | $T_{amb}$<br>= 25°C | $T_{amb}$<br>HIGH | Unit    |
|-------------------------------------------------------------------------------|--------------------------------------------------------|-----------|-------------|------------------|---------------------|-------------------|---------|
| Quiescent device current                                                      | $V_{IL} = 0V$<br>$V_{IH} = V_{DD}$                     |           |             |                  |                     |                   |         |
| Full temperature range                                                        | Outputs open circuit                                   | $I_{DDA}$ | 5,0         | 5,0              | 5,0                 | 150,0             | $\mu A$ |
|                                                                               |                                                        | $I_{DDA}$ | 10,0        | 10,0             | 10,0                | 300,0             | $\mu A$ |
|                                                                               |                                                        | $I_{DDA}$ | 15,0        | 20,0             | 20,0                | 600,0             | $\mu A$ |
| Limited temperature range                                                     |                                                        | $I_{DDA}$ | 5,0         | 20,0             | 20,0                | 150,0             | $\mu A$ |
|                                                                               |                                                        | $I_{DDA}$ | 10,0        | 40,0             | 40,0                | 300,0             | $\mu A$ |
|                                                                               |                                                        | $I_{DDA}$ | 15,0        | 80,0             | 80,0                | 600,0             | $\mu A$ |
| LOW level output voltage at $ I_O  < 1,0\mu A$                                | $V_{IL} = 0V$<br>$V_{IH} = V_{DD}$                     | $V_{OLA}$ | 5,0         | 0,05             | 0,05                | 0,05              | V       |
|                                                                               |                                                        | $V_{OLA}$ | 10,0        | 0,05             | 0,05                | 0,05              | V       |
|                                                                               |                                                        | $V_{OLA}$ | 15,0        | 0,05             | 0,05                | 0,05              | V       |
| HIGH level output voltage at $ I_O  < 1,0\mu A$                               | $V_{IL} = 0V$<br>$V_{IH} = V_{DD}$                     | $V_{OHB}$ | 5,0         | 4,95             | 4,95                | 4,95              | V       |
|                                                                               |                                                        | $V_{OHB}$ | 10,0        | 9,95             | 9,95                | 9,95              | V       |
|                                                                               |                                                        | $V_{OHB}$ | 15,0        | 14,95            | 14,95               | 14,95             | V       |
| LOW level output voltage (for worst case combinations) at $ I_O  < 1,0\mu A$  | $V_{IL} = 1,5V$<br>$V_{IL} = 3,0V$<br>$V_{IL} = 4,0V$  | $V_{OLA}$ | 5,0         | 0,5              | 0,5                 | 0,5               | V       |
|                                                                               |                                                        | $V_{OLA}$ | 10,0        | 1,0              | 1,0                 | 1,0               | V       |
|                                                                               |                                                        | $V_{OLA}$ | 15,0        | 1,5              | 1,5                 | 1,5               | V       |
| HIGH level output voltage (for worst case combinations) at $ I_O  < 1,0\mu A$ | $V_{IH} = 3,5V$<br>$V_{IH} = 7,0V$<br>$V_{IH} = 11,0V$ | $V_{OHB}$ | 5,0         | 4,5              | 4,5                 | 4,5               | V       |
|                                                                               |                                                        | $V_{OHB}$ | 10,0        | 9,0              | 9,0                 | 9,0               | V       |
|                                                                               |                                                        | $V_{OHB}$ | 15,0        | 13,5             | 13,5                | 13,5              | V       |
| Output LOW (sink) current                                                     |                                                        |           |             |                  |                     |                   |         |
| Full temperature range                                                        | $V_O = 0,4V$<br>$V_O = 0,5V$<br>$V_O = 1,5V$           | $I_{OLB}$ | 5,0         | 0,64             | 0,51                | 0,36              | mA      |
|                                                                               |                                                        | $I_{OLB}$ | 10,0        | 1,60             | 1,30                | 0,90              | mA      |
|                                                                               |                                                        | $I_{OLB}$ | 15,0        | 4,20             | 3,40                | 2,40              | mA      |
| Limited temperature range                                                     | $V_O = 0,4V$<br>$V_O = 0,5V$<br>$V_O = 1,5V$           | $I_{OLB}$ | 5,0         | 0,52             | 0,44                | 0,36              | mA      |
|                                                                               |                                                        | $I_{OLB}$ | 10,0        | 1,30             | 1,10                | 0,90              | mA      |
|                                                                               |                                                        | $I_{OLB}$ | 15,0        | 3,60             | 3,00                | 2,40              | mA      |

| Characteristics                                                                                                       | Conditions                                           | Symbol     | $V_{DD}(V)$ | $T_{amb}$<br>LOW | $T_{amb}$<br>= 25°C | $T_{amb}$<br>HIGH | Unit    |
|-----------------------------------------------------------------------------------------------------------------------|------------------------------------------------------|------------|-------------|------------------|---------------------|-------------------|---------|
| Output HIGH (source) current                                                                                          |                                                      |            |             |                  |                     |                   |         |
| Full temperature range                                                                                                | $V_O = 4,6V$                                         | $-I_{OHB}$ | 5,0         | 0,64             | 0,51                | 0,36              | mA      |
|                                                                                                                       | $V_O = 9,5V$                                         | $-I_{OHB}$ | 10,0        | 1,60             | 1,30                | 0,90              | mA      |
|                                                                                                                       | $V_O = 13,5V$                                        | $-I_{OHB}$ | 15,0        | 4,20             | 3,40                | 2,40              | mA      |
| Limited temperature range                                                                                             | $V_O = 4,6V$                                         | $-I_{OHB}$ | 5,0         | 0,52             | 0,44                | 0,36              | mA      |
|                                                                                                                       | $V_O = 9,5V$                                         | $-I_{OHB}$ | 10,0        | 1,30             | 1,10                | 0,90              | mA      |
|                                                                                                                       | $V_O = 13,5V$                                        | $-I_{OHB}$ | 15,0        | 3,60             | 3,00                | 2,40              | mA      |
| Input leakage current                                                                                                 | $V_{IL} = 0V$<br>$V_{IH} = V_{DD}$                   |            |             |                  |                     |                   |         |
| Full temperature range                                                                                                |                                                      | $ I_{IA} $ | 15,0        | 0,10             | 0,10                | 1,00              | $\mu A$ |
| Limited temperature range                                                                                             |                                                      | $ I_{IA} $ | 15,0        | 0,30             | 0,30                | 1,00              | $\mu A$ |
| Input capacitance per unit load (Any input)                                                                           | $V_I = 0V$<br>$f = 1MHz$                             | $C_{IA}$   | -           | -                | 7,5                 | -                 | pF      |
| Noise margin at LOW level output (equal to the difference between $V_{IL}$ and $V_{OL}$ for worst case combinations)  |                                                      | $V_{NLB}$  | 5,0         | 1,0              | 1,0                 | 1,0               | V       |
|                                                                                                                       |                                                      | $V_{NLB}$  | 10,0        | 2,0              | 2,0                 | 2,0               | V       |
|                                                                                                                       |                                                      | $V_{NLB}$  | 15,0        | 2,5              | 2,5                 | 2,5               | V       |
| Noise margin at HIGH level output (equal to the difference between $V_{IH}$ and $V_{OH}$ for worst case combinations) |                                                      | $V_{NHB}$  | 5,0         | 1,0              | 1,0                 | 1,0               | V       |
|                                                                                                                       |                                                      | $V_{NHB}$  | 10,0        | 2,0              | 2,0                 | 2,0               | V       |
|                                                                                                                       |                                                      | $V_{NHB}$  | 15,0        | 2,5              | 2,5                 | 2,5               | V       |
| Propagation and Transition Times                                                                                      | $C_L = 50pF$<br>(Test conditions as in Sub-group A5) |            |             |                  |                     |                   |         |

| Characteristics                                                                                        | Conditions | Symbol              | V <sub>DD</sub> (V) | T <sub>amb</sub><br>LOW | T <sub>amb</sub><br>= 25°C | T <sub>amb</sub><br>HIGH | Unit |
|--------------------------------------------------------------------------------------------------------|------------|---------------------|---------------------|-------------------------|----------------------------|--------------------------|------|
| Propagation Delay Time<br>HIGH to LOW and<br>LOW to HIGH level<br>Data Input to Q <sub>n</sub> (1)*    |            | t <sub>PHLA</sub> / | 5,0                 | -                       | 400,0                      | -                        | ns   |
|                                                                                                        |            | t <sub>PLHA</sub>   | 10,0                | -                       | 150,0                      | -                        | ns   |
|                                                                                                        |            |                     | 15,0                | -                       | 100,0                      | -                        | ns   |
| Propagation Delay Time<br>HIGH to LOW and<br>LOW to HIGH level<br>Write Disable to Q <sub>n</sub> (2)* |            | t <sub>PHLA</sub> / | 5,0                 | -                       | 400,0                      | -                        | ns   |
|                                                                                                        |            | t <sub>PLHA</sub>   | 10,0                | -                       | 160,0                      | -                        | ns   |
|                                                                                                        |            |                     | 15,0                | -                       | 100,0                      | -                        | ns   |
| Propagation Delay Time<br>HIGH to LOW and LOW<br>to HIGH level<br>Address Input to Q <sub>n</sub> (9)* |            | t <sub>PHLA</sub> / | 5,0                 | -                       | 450,0                      | -                        | ns   |
|                                                                                                        |            | t <sub>PLHA</sub>   | 10,0                | -                       | 200,0                      | -                        | ns   |
|                                                                                                        |            |                     | 15,0                | -                       | 150,0                      | -                        | ns   |
| Propagation Delay Time<br>HIGH to LOW level<br>Reset to Q <sub>n</sub> (3)*                            |            | t <sub>PHLA</sub>   | 5,0                 | -                       | 350,0                      | -                        | ns   |
|                                                                                                        |            | t <sub>PHLA</sub>   | 10,0                | -                       | 160,0                      | -                        | ns   |
|                                                                                                        |            | t <sub>PHLA</sub>   | 15,0                | -                       | 130,0                      | -                        | ns   |
| Output Transition Time<br>HIGH to LOW and LOW<br>to HIGH level<br>Q <sub>n</sub><br>Any output         |            | t <sub>THLA</sub> / | 5,0                 | -                       | 200,0                      | -                        | ns   |
|                                                                                                        |            | t <sub>TLHA</sub>   | 10,0                | -                       | 100,0                      | -                        | ns   |
|                                                                                                        |            |                     | 15,0                | -                       | 80,0                       | -                        | ns   |
| Pulse Width<br>Data (4)*                                                                               |            | t <sub>PWDB</sub>   | 5,0                 | -                       | 200,0                      | -                        | ns   |
|                                                                                                        |            | t <sub>PWDB</sub>   | 10,0                | -                       | 100,0                      | -                        | ns   |
|                                                                                                        |            | t <sub>PWDB</sub>   | 15,0                | -                       | 80,0                       | -                        | ns   |
| Pulse Width<br>Address (8)*                                                                            |            | t <sub>PWAB</sub>   | 5,0                 | -                       | 400,0                      | -                        | ns   |
|                                                                                                        |            | t <sub>PWAB</sub>   | 10,0                | -                       | 200,0                      | -                        | ns   |
|                                                                                                        |            | t <sub>PWAB</sub>   | 15,0                | -                       | 125,0                      | -                        | ns   |
| Pulse Width<br>Reset (5)*                                                                              |            | t <sub>PWRB</sub>   | 5,0                 | -                       | 150,0                      | -                        | ns   |
|                                                                                                        |            | t <sub>PWRB</sub>   | 10,0                | -                       | 75,0                       | -                        | ns   |
|                                                                                                        |            | t <sub>PWRB</sub>   | 15,0                | -                       | 50,0                       | -                        | ns   |

NOTE In addition to the above characteristics, a WRITE DISABLE ON time (the time that the WRITE DISABLE is at HIGH level) must be observed during an address change for the total time that the external address lines A0, A1 and A2 are settling to a stable level i.e. WD may go LOW after the transition of the last changing address line as shown in Figure (4), to prevent a wrong cell from being addressed.

\*Timing diagram (Figure 4) reference

| Characteristics                              | Conditions | Symbol             | V <sub>DD</sub> (V) | T <sub>amb</sub><br>LOW | T <sub>amb</sub><br>= 25°C | T <sub>amb</sub><br>HIGH | Unit |
|----------------------------------------------|------------|--------------------|---------------------|-------------------------|----------------------------|--------------------------|------|
| Set-Up Time<br>Data to Write<br>Disable (6)* |            | t <sub>PWSTB</sub> | 5,0                 | -                       | 100,0                      | -                        | ns   |
|                                              |            | t <sub>PWSTB</sub> | 10,0                | -                       | 50,0                       | -                        | ns   |
|                                              |            | t <sub>PWSTB</sub> | 15,0                | -                       | 35,0                       | -                        | ns   |
| Hold Time<br>Data to Write<br>Disable (7)*   |            | t <sub>PWHB</sub>  | 5,0                 | -                       | 150,0                      | -                        | ns   |
|                                              |            | t <sub>PWHB</sub>  | 10,0                | -                       | 75,0                       | -                        | ns   |
|                                              |            | t <sub>PWHB</sub>  | 15,0                | -                       | 50,0                       | -                        | ns   |

NOTE In addition to the above characteristics, a WRITE DISABLE ON time (the time that the WRITE DISABLE is at HIGH level) must be observed during an address change for the total time that the external address lines A<sub>0</sub>, A<sub>1</sub> and A<sub>2</sub> are settling to a stable level i.e. WD may go LOW after the transition of the last changing address line as shown in Figure (4), to prevent a wrong cell from being addressed.

\*Timing diagram (Figure 4) reference

#### Terminal identification

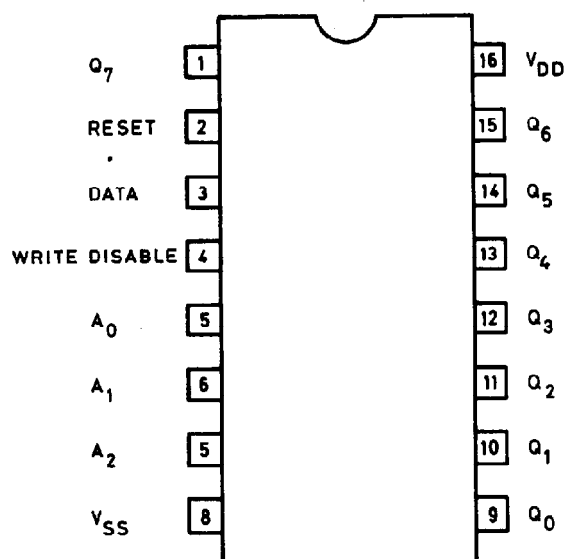


Figure 1

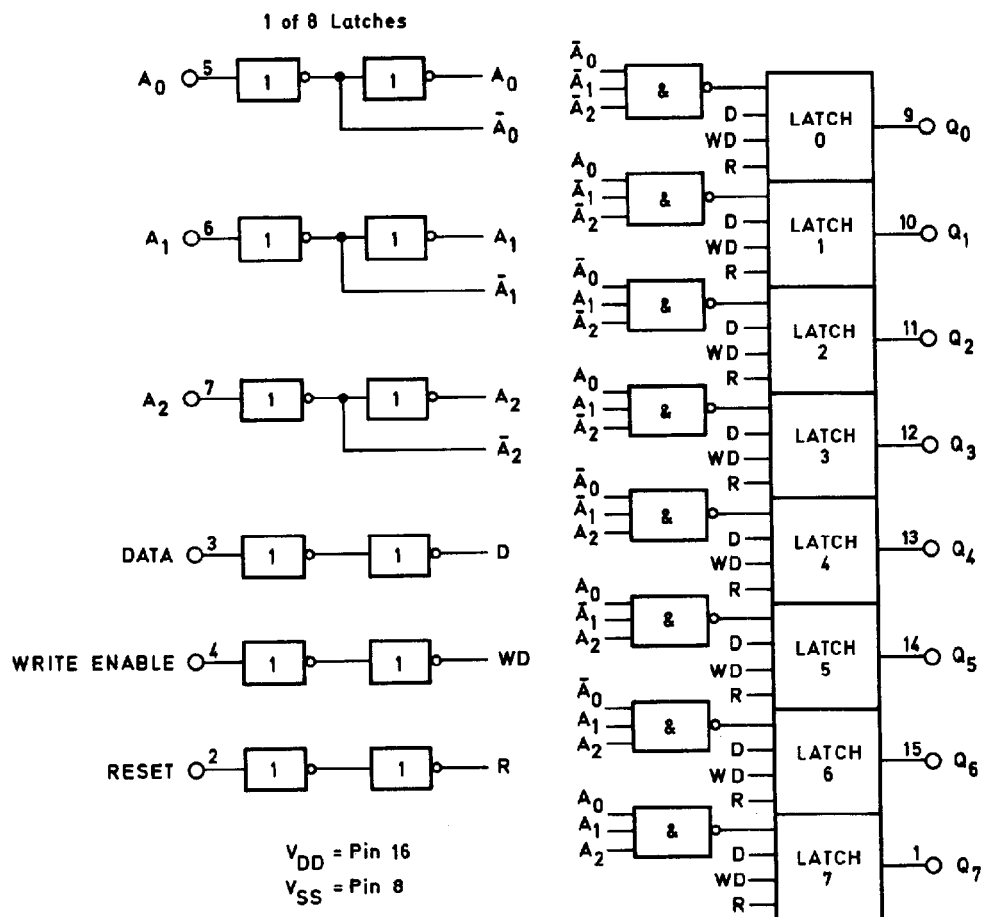
Function Table

Table 1

| FUNCTION<br>TYPE<br>(See Fig. 3) | MODE SELECTION |   |                                       |                      |
|----------------------------------|----------------|---|---------------------------------------|----------------------|
|                                  | WD             | R | ADDRESSED LATCH                       | UNADDRESSED LATCH    |
| A                                | L              | L | Follows Data                          | Holds Previous Level |
| B                                | L              | H | Follows Data                          | Reset to "L"         |
|                                  |                |   | (Active HIGH 8-Channel Demultiplexer) |                      |
| C                                | H              | L | Holds Previous Level                  |                      |
| D                                | H              | H | Reset to "L"                          | Reset to "L"         |

H = HIGH level  
L = LOW level  
R = Reset  
WD = Write Disable

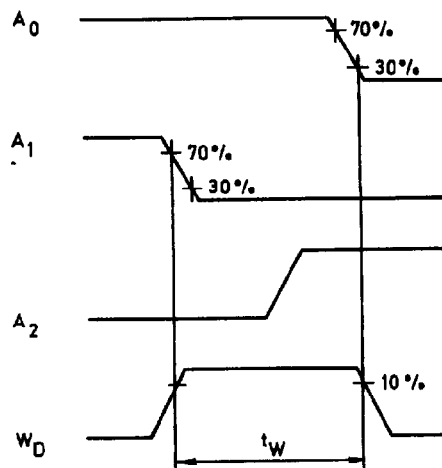
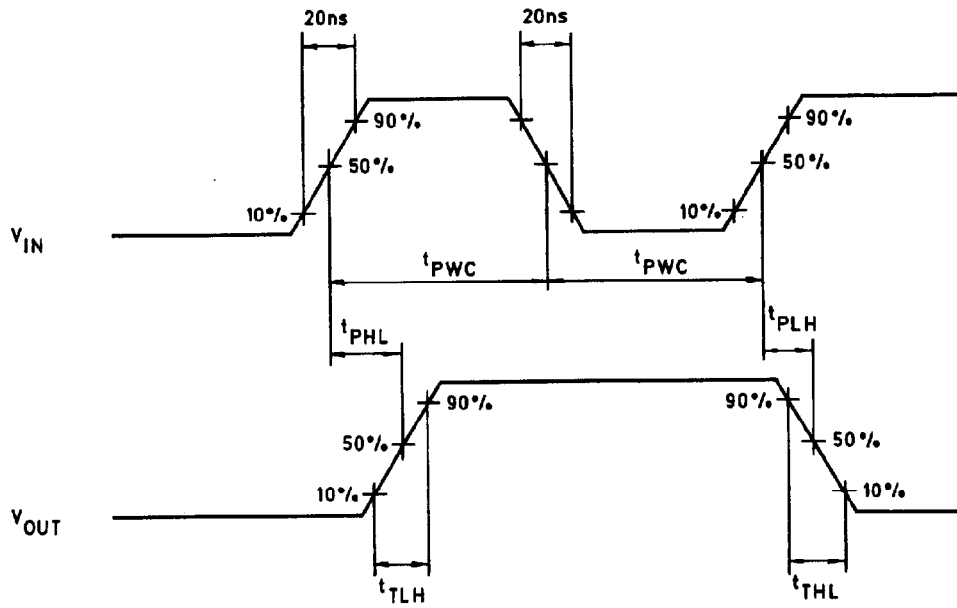
Typical logic diagram



This is a graphic representation, not a circuit diagram

Figure 2

# Switching time waveforms



DEFINITION OF WRITE DISABLE ON TIME

Figure 3