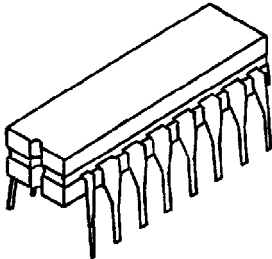


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90 104 - 157 ISSUE 1 DECEMBER 1981  Page 1 of 26 pages
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 4511B SEE PD 9002 AND CECC 00 200 For ordering information see page 11
Outline not to scale: Isometric projection Marking information see page 10  For detail dimensions see IEC 191-2 (A50C)	BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER SILICON COMPLEMENTARY MOS. WITH (B) BUFFERED OUTPUTS AND CAVITY PACKAGING. Assessment levels R, S, T and V and optional screening categories A, B, C and D

CAUTION: THESE ARE STATIC SENSITIVE DEVICES - See clause 1.11.

1. Limiting conditions of use (not for inspection purposes)

All voltages referenced to V_{SS}

1.1	Maximum supply voltage, positive	V_{DD}	+18,0V
1.2	Maximum supply voltage, negative	V_{DD}	-0,5V
1.3	Maximum positive input voltage	V_I	V_{DD} +0,5V
1.4	Maximum negative input voltage	V_I	-0,5V

Refer to Qualified Products List PD 9002 and/or CECC 00 200
 for details of manufacturers approved to this specification

1. Limiting conditions of use (contd)

- | | | | |
|---------|--|-----------|--------------------------------|
| 1.5 | Maximum power dissipation, per package | P_{D1} | 200,0mW |
| | per output | P_{D2} | 28,57mW |
| 1.6 | Maximum continuous current into any input. | $ I_I $ | 10,0mA |
| 1.7 | Maximum continuous current into any output. | $ I_O $ | 10,0mA |
| 1.8 | Operating temperature range | T_{amb} | |
| | | Full | -55 to +125°C |
| | | Limited | -40 to + 85°C |
| 1.9 | Storage temperature range | T_{stg} | -65 to +150°C |
| 1.10 | Transient energy rating | | 400V at 100pF
through 1,5kΩ |
| 1.11 | <u>Recommended handling precautions</u> | | |
| 1.11.1 | Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method. | | |
| 1.11.2 | Use grounded tip soldering irons. | | |
| 1.11.3 | Ground all test equipment. | | |
| 1.11.4 | Connect all unused device inputs to V_{DD} or V_{SS} . | | |
| 1.11.5 | PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations. | | |
| 1.11.6 | Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices. | | |
| 1.11.7 | Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during inspection or handling. | | |
| 1.11.8 | When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage, 'Dummy connectors' should be used to electrically short all PC board terminals together. | | |
| 1.11.9 | Switch off power supply before inserting or removing devices from circuits. | | |
| 1.11.10 | Disconnect all low impedance equipment and input signals from the device before d.c. power supplies are switched off. | | |

2. Recommended conditions of use and associated characteristics (not for inspection purposes)

These apply over the operating temperature range unless otherwise stated. All voltages referenced to V_{SS} .

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Quiescent device current	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range	Outputs open circuit	I_{DDA}	5,0	5,0	5,0	150,0	μA
		I_{DDA}	10,0	10,0	10,0	300,0	μA
		I_{DDA}	15,0	15,0	20,0	600,0	μA
Limited temperature range		I_{DDA}	5,0	20,0	20,0	150,0	μA
		I_{DDA}	10,0	40,0	40,0	300,0	μA
		I_{DDA}	15,0	80,0	80,0	600,0	μA
LOW level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OLA}	5,0	0,05	0,05	0,05	V
		V_{OLA}	10,0	0,05	0,05	0,05	V
		V_{OLA}	15,0	0,05	0,05	0,05	V
HIGH level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OHB}	5,0	4,95	4,05	4,95	V
		V_{OHB}	10,0	9,95	9,95	9,95	V
		V_{OHB}	15,0	14,95	14,95	14,95	V
LOW level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IL} = 1,5V$ $V_{IL} = 3,0V$ $V_{IL} = 4,0V$	V_{OLA}	5,0	0,5	0,5	0,5	V
		V_{OLA}	10,0	1,0	1,0	1,0	V
		V_{OLA}	15,0	1,5	1,5	1,5	V
HIGH level output voltage (for worst case combinations)							
Full temperature range							
$-I_{OH} = 0mA$	$V_{IH} = 3,5V$	V_{OHB}	5,0	4,1	4,1	4,1	V
$-I_{OH} = 10,0mA$		V_{OHB}	5,0	3,9	3,9	3,5	V
$-I_{OH} = 20,0mA$		V_{OHB}	5,0	3,4	3,4	3,0	V
$-I_{OH} = 0mA$	$V_{IH} = 7,0V$	V_{OHB}	10,0	9,1	9,1	9,1	V
$-I_{OH} = 10,0mA$		V_{OHB}	10,0	9,0	9,0	8,6	V
$-I_{OH} = 20,0mA$		V_{OHB}	10,0	8,6	8,6	8,2	V
$-I_{OH} = 0mA$	$V_{IH} = 11,0V$	V_{OHB}	15,0	14,1	14,1	14,1	V
$-I_{OH} = 10,0mA$		V_{OHB}	15,0	14,0	14,0	13,6	V
$-I_{OH} = 20,0mA$		V_{OHB}	15,0	13,6	13,6	13,2	V

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25°C	T _{amb} HIGH	Unit
HIGH level output voltage (for worst case combinations) (contd)							
Limited temperature range							
-I _{OH} = 0mA	V _{IH} = 3,5V	V _{OHB}	5,0	4,1	4,1	4,1	V
-I _{OH} = 10,0mA		V _{OHB}	5,0	3,6	3,6	3,3	V
-I _{OH} = 20,0mA		V _{OHB}	5,0	2,8	2,8	2,5	V
-I _{OH} = 0mA	V _{IH} = 7,0V	V _{OHB}	10,0	9,10	9,10	9,1	V
-I _{OH} = 10,0mA		V _{OHB}	10,0	8,75	8,75	8,45	V
-I _{OH} = 20,0mA		V _{OHB}	10,0	8,10	8,10	7,8	V
-I _{OH} = 0mA	V _{IH} = 11,0V	V _{OHB}	15,0	14,10	14,10	14,10	V
-I _{OH} = 10,0mA		V _{OHB}	15,0	13,75	13,75	13,75	V
-I _{OH} = 20,0mA		V _{OHB}	15,0	13,10	13,10	12,80	V
Output LOW (sink) current							
Full temperature range	V _O = 0,4V	I _{OLB}	5,0	0,64	0,51	0,36	mA
	V _O = 0,5V	I _{OLB}	10,0	1,60	1,30	0,90	mA
	V _O = 1,5V	I _{OLB}	15,0	4,20	3,40	2,40	mA
Limited temperature range	V _O = 0,4V	I _{OLB}	5,0	0,52	0,44	0,36	mA
	V _O = 0,5V	I _{OLB}	10,0	1,30	1,10	0,90	mA
	V _O = 1,5V	I _{OLB}	15,0	3,60	3,00	2,40	mA
Output HIGH (source) current							
Full temperature range	V _O = 4,6V	-I _{OHB}	5,0	0,52	0,44	0,36	mA
	V _O = 9,5V	-I _{OHB}	10,0	1,30	1,10	0,90	mA
	V _O = 13,5V	-I _{OHB}	15,0	3,60	3,00	2,40	mA
Limited temperature range	V _O = 4,6V	-I _{OHB}	5,0	0,25	0,2	0,14	mA
	V _O = 9,5V	-I _{OHB}	10,0	0,62	0,5	0,35	mA
	V _O = 13,5V	-I _{OHB}	15,0	1,80	1,5	1,10	mA
Input leakage current	V _{IL} = 0V V _{IH} = V _{DD}						
Full temperature range		I _{IA}	15,0	0,10	0,10	1,00	μA
Limited temperature range		I _{IA}	15,0	0,30	0,30	1,00	μA

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25°C	T _{amb} HIGH	Unit
Input capacitance per unit load (Any input)	V _I = 0V f = 1MHz	C _{IA}	-	-	7,5	-	pF
Noise margin at LOW level output (equal to the difference between V _{IL} and V _{OL} for worst case combinations)		V _{NLB}	5,0	1,0	1,0	1,0	V
		V _{NLB}	10,0	2,0	2,0	2,0	V
		V _{NLB}	15,0	2,5	2,5	2,5	V
Noise margin at HIGH level output (equal to the difference between V _{IH} and V _{OH} for worst case combinations)		V _{NHB}	5,0	1,0	1,0	1,0	V
		V _{NHB}	10,0	2,0	2,0	2,0	V
		V _{NHB}	15,0	2,5	2,5	2,5	V
Propagation and Transition Times	C _L = 50pF (Test conditions as in Sub-group A5)						
Transition Time LOW to HIGH level		t _{TLHA}	5,0	-	100,0	-	ns
		t _{TLHA}	10,0	-	75,0	-	ns
		t _{TLHA}	15,0	-	65,0	-	ns
Transition Time HIGH to LOW level		t _{THLA}	5,0	-	310,0	-	ns
		t _{THLA}	10,0	-	185,0	-	ns
		t _{THLA}	15,0	-	160,0	-	ns
Data Propagation Delay Time LOW to HIGH level		t _{PLHA}	5,0	-	1320,0	-	ns
		t _{PLHA}	10,0	-	520,0	-	ns
		t _{PLHA}	15,0	-	360,0	-	ns
Data Propagation Delay Time HIGH to LOW level		t _{PHLA}	5,0	-	1440,0	-	ns
		t _{PHLA}	10,0	-	580,0	-	ns
		t _{PHLA}	15,0	-	400,0	-	ns
Blank Propagation Delay Time LOW to HIGH level		t _{PLHA}	5,0	-	800,0	-	ns
		t _{PLHA}	10,0	-	350,0	-	ns
		t _{PLHA}	15,0	-	300,0	-	ns
Blank Propagation Delay Time HIGH to LOW level		t _{PHLA}	5,0	-	970,0	-	ns
		t _{PHLA}	10,0	-	400,0	-	ns
		t _{PHLA}	15,0	-	320,0	-	ns

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25°C	T _{amb} HIGH	Unit
Lamp Test Propagation Delay Time HIGH to LOW and LOW to HIGH level		t _{PHLA} /	5,0	-	625,0	-	ns
		t _{PLHA}	10,0	-	250,0	-	ns
			15,0	-	180,0	-	ns
Set-Up Time		t _{PWSTB}	5,0	-	180,0	-	ns
		t _{PWSTB}	10,0	-	76,0	-	ns
		t _{PWSTB}	15,0	-	40,0	-	ns
Hold Time		t _{PWHB}	5,0	-	0	-	ns
		t _{PWHB}	10,0	-	0	-	ns
		t _{PWHB}	15,0	-	0	-	ns
Latch Enable Pulse Width		t _{PWLB}	5,0	-	520,0	-	ns
		t _{PWLB}	10,0	-	220,0	-	ns
		t _{PWLB}	15,0	-	130,0	-	ns

Terminal identification

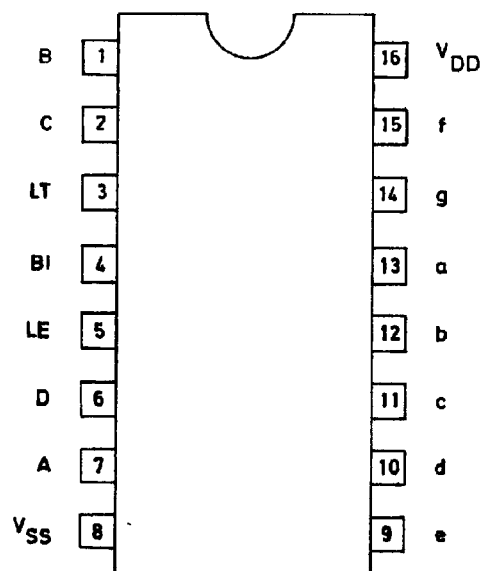
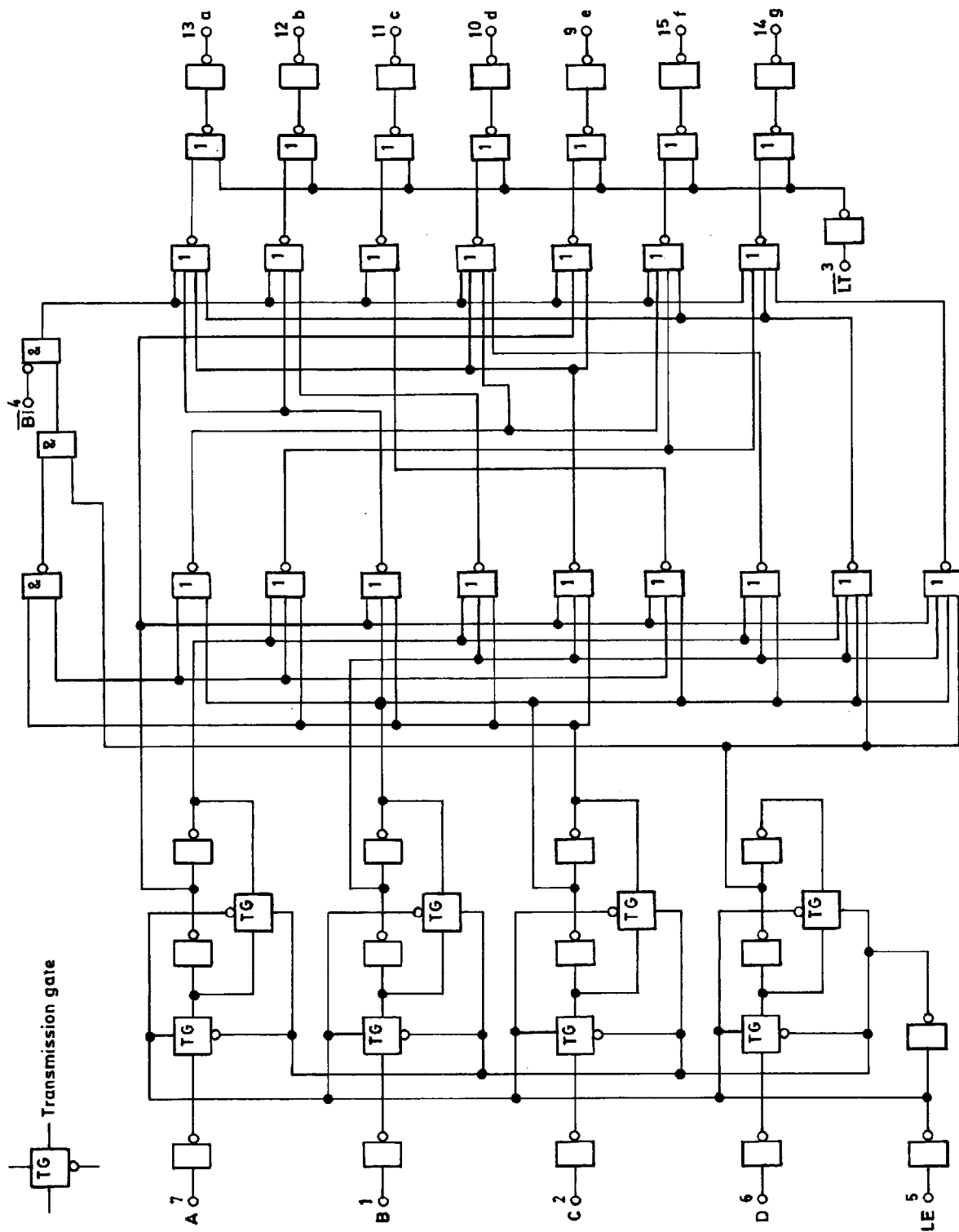


Figure 1

Typical logic diagram



This is a graphic representation, not a circuit diagram

Figure 2