

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 AND

BS CECC 90 104 - 171

ISSUE 1

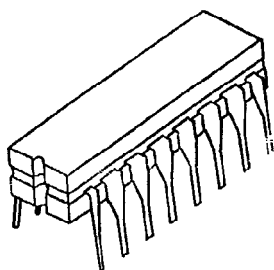
DECEMBER 1981



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ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:BS CECC 90 000 : 1976
BS CECC 90 100 : 1977

MANUFACTURERS TYPE NUMBER

4018BSEE PD 9002 AND CECC 00 200
For ordering information
see page 11Outline not to scale: Isometric projection
Marking information see page 10PRESETTABLE DIVIDE-BY-N
COUNTERSILICON COMPLEMENTARY MOS.
WITH (B) BUFFERED OUTPUTS AND
CAVITY PACKAGING.

For detail dimensions see IEC 191-2 (A50C)

Assessment levels
R, S, T and V
and optional screening
categories A, B, C and D**CAUTION: THESE ARE STATIC SENSITIVE DEVICES - See clause 1.11**1. Limiting conditions of use (not for inspection purposes)All voltages referenced to V_{SS}

1.1	Maximum supply voltage, positive	V_{DD}	+18,0V
1.2	Maximum supply voltage, negative	V_{DD}	-0,5V
1.3	Maximum positive input voltage	V_I	V_{DD} +0,5V
1.4	Maximum negative input voltage	V_I	-0,5V

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1. Limiting conditions of use (contd)

1.5	Maximum power dissipation, per package	P_{D1}	200,0mW
	per output	P_{D2}	40,0mW
1.6	Maximum continuous current into any input.	$ I_I $	10,0mA
1.7	Maximum continuous current into any output.	$ I_O $	10,0mA
1.8	Operating temperature range	T_{amb}	
		Full	-55 to +125°C
		Limited	-40 to + 85°C
1.9	Storage temperature range	T_{stg}	-65 to +150°C
1.10	Transient energy rating		400V at 100pF through 1,5kΩ

1.11 Recommended handling precautions

- 1.11.1 Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method.
- 1.11.2 Use grounded tip soldering irons.
- 1.11.3 Ground all test equipment.
- 1.11.4 Connect all unused device inputs to V_{DD} or V_{SS} .
- 1.11.5 PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations.
- 1.11.6 Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices.
- 1.11.7 Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during inspection or handling.
- 1.11.8 When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage, 'Dummy connectors' should be used to electrically short all PC board terminals together.
- 1.11.9 Switch off power supply before inserting or removing devices from circuits.
- 1.11.10 Disconnect all low impedance equipment and input signals from the device before d.c. power supplies are switched off.

2. Recommended conditions of use and associated characteristics (not for inspection purposes)

These apply over the operating temperature range unless otherwise stated. All voltages referenced to V_{SS} .

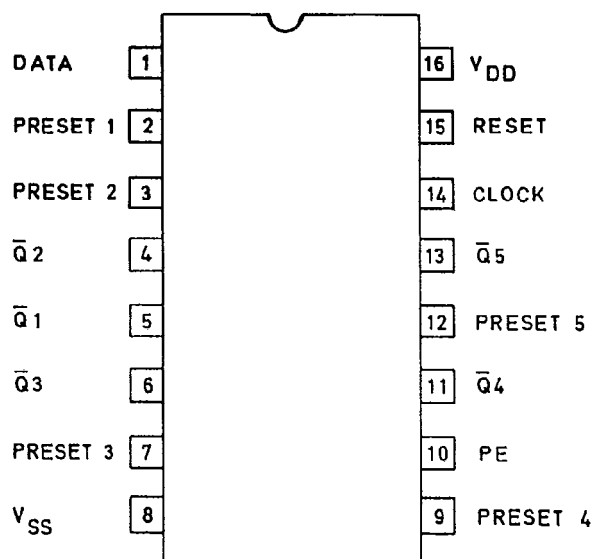
Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Quiescent device current	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range	Outputs open circuit	I_{DDA}	5,0	5,0	5,0	150,0	μA
		I_{DDA}	10,0	10,0	10,0	300,0	μA
		I_{DDA}	15,0	20,0	20,0	600,0	μA
		I_{DDA}	5,0	20,0	20,0	150,0	μA
		I_{DDA}	10,0	40,0	40,0	300,0	μA
		I_{DDA}	15,0	80,0	80,0	600,0	μA
Limited temperature range		I_{DDA}	5,0	20,0	20,0	150,0	μA
		I_{DDA}	10,0	40,0	40,0	300,0	μA
		I_{DDA}	15,0	80,0	80,0	600,0	μA
LOW level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OLA}	5,0	0,05	0,05	0,05	V
		V_{OLA}	10,0	0,05	0,05	0,05	V
		V_{OLA}	15,0	0,05	0,05	0,05	V
HIGH level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OHB}	5,0	4,95	4,95	4,95	V
		V_{OHB}	10,0	9,95	9,95	9,95	V
		V_{OHB}	15,0	14,95	14,95	14,95	V
LOW level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IL} = 1,5V$ $V_{IL} = 3,0V$ $V_{IL} = 4,0V$	V_{OLA}	5,0	0,5	0,5	0,5	V
		V_{OLA}	10,0	1,0	1,0	1,0	V
		V_{OLA}	15,0	1,5	1,5	1,5	V
HIGH level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IH} = 3,5V$ $V_{IH} = 7,0V$ $V_{IH} = 11,0V$	V_{OHB}	5,0	4,5	4,5	4,5	V
		V_{OHB}	10,0	9,0	9,0	9,0	V
		V_{OHB}	15,0	13,5	13,5	13,5	V
Output LOW (sink) current							
Full temperature range	$V_O = 0,4V$ $V_O = 0,5V$ $V_O = 1,5V$	I_{OLB}	5,0	0,64	0,51	0,36	mA
		I_{OLB}	10,0	1,60	1,30	0,90	mA
		I_{OLB}	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_O = 0,4V$ $V_O = 0,5V$ $V_O = 1,5V$	I_{OLB}	5,0	0,52	0,44	0,36	mA
		I_{OLB}	10,0	1,30	1,10	0,90	mA
		I_{OLB}	15,0	3,60	3,00	2,40	mA

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Output HIGH (source) current							
Full temperature range	$V_O = 4,6V$	$-I_{OHB}$	5,0	0,64	0,51	0,36	mA
	$V_O = 9,5V$	$-I_{OHB}$	10,0	1,60	1,30	0,90	mA
	$V_O = 13,5V$	$-I_{OHB}$	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_O = 4,6V$	$-I_{OHB}$	5,0	0,52	0,44	0,36	mA
	$V_O = 9,5V$	$-I_{OHB}$	10,0	1,30	1,10	0,90	mA
	$V_O = 13,5V$	$-I_{OHB}$	15,0	3,60	3,00	2,40	mA
Input leakage current	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range		$ I_{IA} $	15,0	0,10	0,10	1,00	μA
Limited temperature range		$ I_{IA} $	15,0	0,30	0,30	1,00	μA
Input capacitance per unit load (Any input)	$V_I = 0V$ $f = 1MHz$	C_{IA}	-	-	7,5	-	pF
Noise margin at LOW level output (equal to the difference between V_{IL} and V_{OL} for worst case combinations)		V_{NLB} V_{NLB} V_{NLB}	5,0 10,0 15,0	1,0 2,0 2,5	1,0 2,0 2,5	1,0 2,0 2,5	V V V
Noise margin at HIGH level output (equal to the difference between V_{IH} and V_{OH} for worst case combinations)		V_{NHB} V_{NHB} V_{NHB}	5,0 10,0 15,0	1,0 2,0 2,5	1,0 2,0 2,5	1,0 2,0 2,5	V V V
Propagation and Transition Times	$C_L = 50pF$ (Test conditions as in Sub-group A5)						

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25°C	T _{amb} HIGH	Unit
Propagation Delay Time HIGH to LOW and LOW to HIGH level Clock to $\bar{Q}$		$t_{PHLA}/$ t_{PLHA}	5,0	-	620,0	-	ns
			10,0	-	240,0	-	ns
			15,0	-	170,0	-	ns
Propagation Delay Time HIGH to LOW and LOW to HIGH level Reset to $\bar{Q}$		$t_{PHLA}/$ t_{PLHA}	5,0	-	740,0	-	ns
			10,0	-	300,0	-	ns
			15,0	-	200,0	-	ns
Propagation Delay Time HIGH to LOW and LOW to HIGH level Preset Enable to $\bar{Q}$		$t_{PHLA}/$ t_{PLHA}	5,0	-	740,0	-	ns
			10,0	-	300,0	-	ns
			15,0	-	200,0	-	ns
Transition Time HIGH to LOW and LOW to HIGH level		$t_{THLA}/$ t_{TLHA}	5,0	-	200,0	-	ns
			10,0	-	100,0	-	ns
			15,0	-	80,0	-	ns
Set-up Time Data (Pin 1) to Clock		t_{PWSTB} t_{PWSTB} t_{PWSTB}	5,0	-	200,0	-	ns
			10,0	-	100,0	-	ns
			15,0	-	80,0	-	ns
Set-up Time Preset Inputs to Preset Enable		t_{PWSTB} t_{PWSTB} t_{PWSTB}	5,0	-	200,0	-	ns
			10,0	-	100,0	-	ns
			15,0	-	80,0	-	ns
Data (Preset Inputs) to Preset Enable Hold Time		t_{PWHB} t_{PWHB} t_{PWHB}	5,0	-	540,0	-	ns
			10,0	-	500,0	-	ns
			15,0	-	480,0	-	ns
Clock Pulse Width		t_{PWCB} t_{PWCB} t_{PWCB}	5,0	-	400,0	-	ns
			10,0	-	200,0	-	ns
			15,0	-	160,0	-	ns
Reset or Preset Enable Pulse Width		$t_{PWRB}/$ t_{PWEB}	5,0	-	290,0	-	ns
			10,0	-	130,0	-	ns
		$t_{PWRB}/$ t_{PWEB}	10,0	-	130,0	-	ns
			15,0	-	110,0	-	ns
		$t_{PWRB}/$ t_{PWEB}	15,0	-	110,0	-	ns

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Maximum Clock Rise and Fall Times		t_{rA}, t_{fA}	5,0	-	20,0	-	ms
		t_{rA}, t_{fA}	10,0	-	20,0	-	ms
		t_{rA}, t_{fA}	15,0	-	20,0	-	ms
Clock Pulse Frequency		$f_{max.A}$	5,0	-	1,25	-	MHz
		$f_{max.A}$	10,0	-	3,25	-	MHz
		$f_{max.A}$	15,0	-	4,00	-	MHz

Terminal identification



PE = Preset Enable

Figure 1

Function Table

Table 1

CLOCK	RESET	PRESET ENABLE	PRESETS 1-5 ENABLE	$\overline{Q}_n$
	L	L	X	$\overline{Q}_n$
	L	L	X	$\overline{D}_{n*}$
X	L	H	L	H
X	L	H	H	L
X	H	X	X	H

*Dn is the data input for that stage.
Stage 1 has data input brought out to
Pin 1

H = HIGH level
L = LOW level
X = Level irrelevant

Switching time waveforms

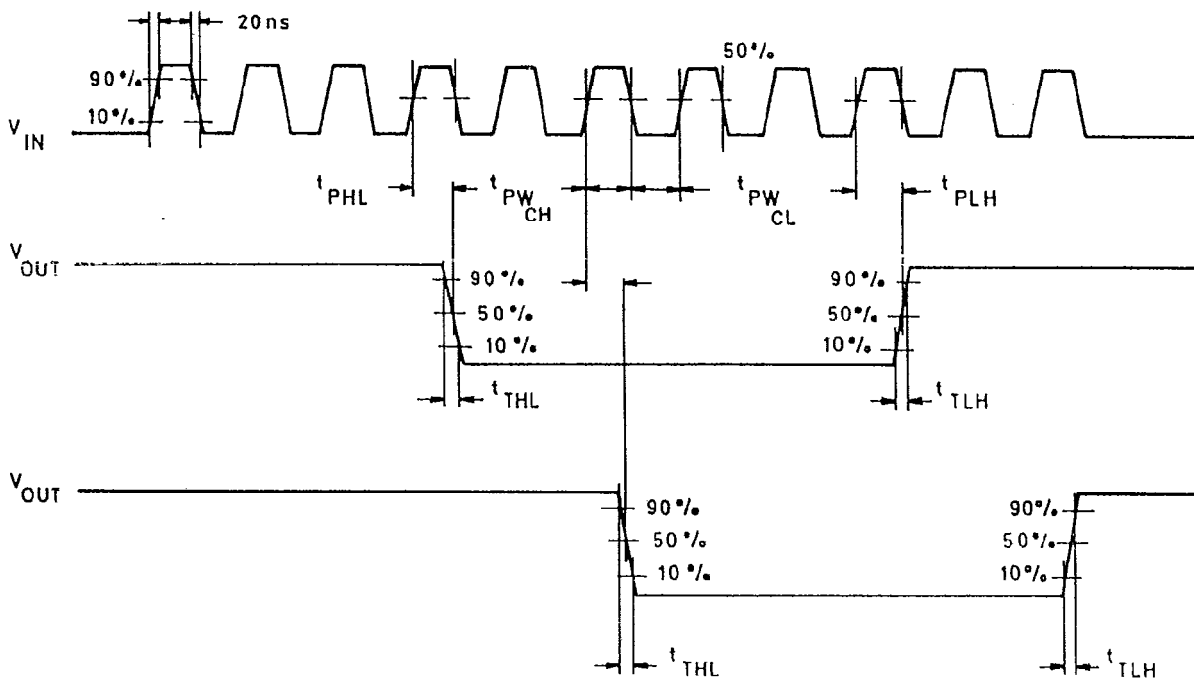
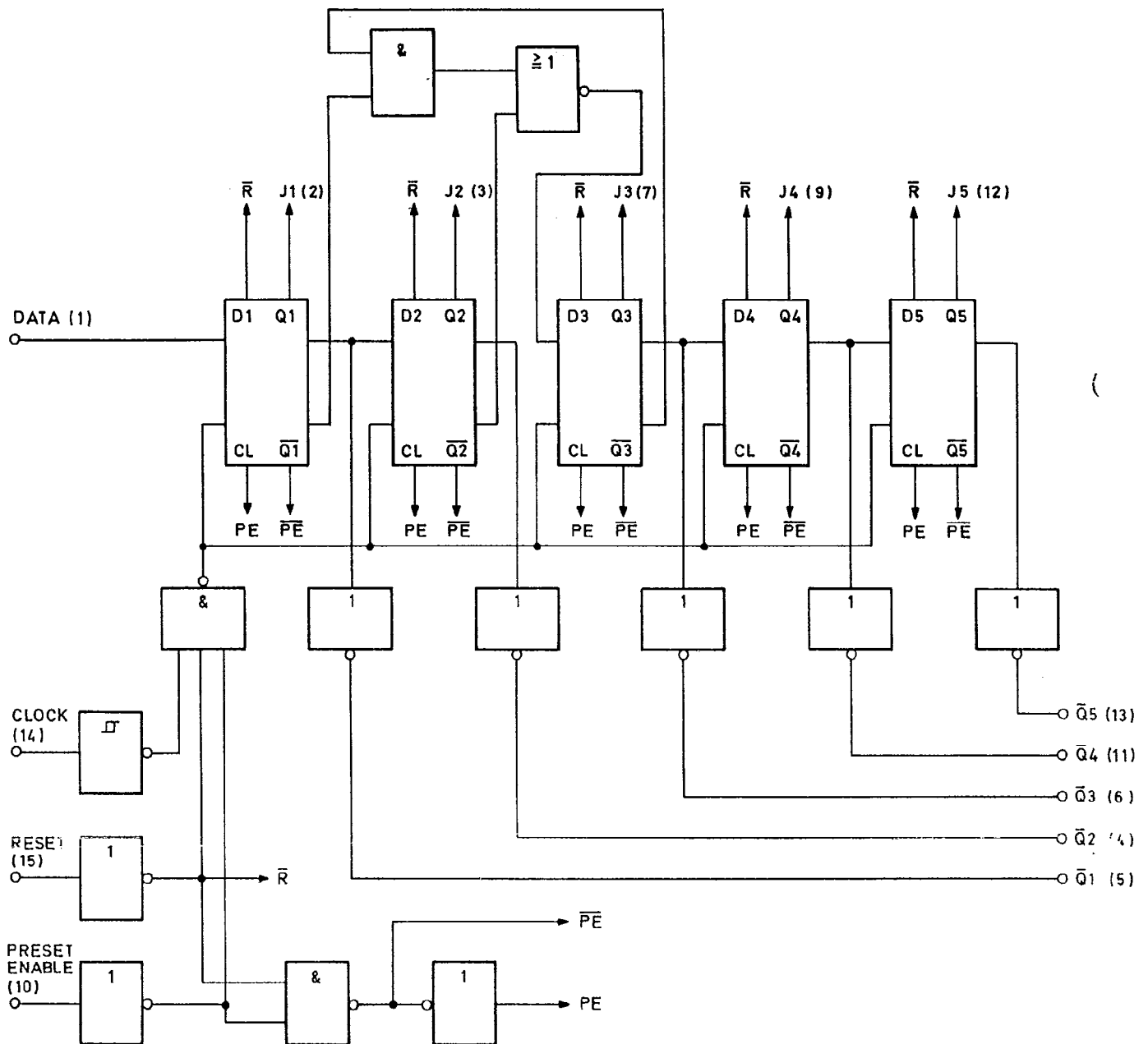


Figure 2

Typical logic diagram



This is a graphic representation, not a circuit diagram

Figure 3