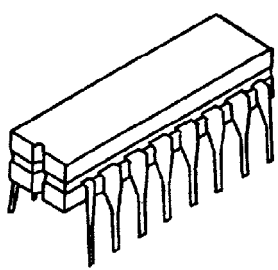


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90 104 - 179
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	ISSUE 1  DECEMBER 1981 Page 1 of 26 pages
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	MANUFACTURERS TYPE NUMBER 4538B
Outline not to scale: Isometric projection Marking information see page 9  For detail dimensions see IEC 191-2 (A50C)	SEE PD 9002 AND CECC 00 200 For ordering information see page 10
	DUAL, RETRIGGERABLE, RESETTABLE MONOSTABLE MULTIVIBRATOR
	SILICON COMPLEMENTARY MOS. WITH (B) BUFFERED OUTPUTS AND CAVITY PACKAGING.
	Assessment levels R, S, T and V and optional screening categories A, B, C and D

CAUTION: THESE ARE STATIC SENSITIVE DEVICES - See clause 1.11

1. Limiting conditions of use (not for inspection purposes)

All voltages referenced to V_{SS}

1.1	Maximum supply voltage, positive	V_{DD}	+18,0V
1.2	Maximum supply voltage, negative	V_{DD}	-0,5V
1.3	Maximum positive input voltage	V_I	V_{DD} +0,5V
1.4	Maximum negative input voltage	V_I	-0,5V

Refer to Qualified Products List PD 9002 and/or CECC 00 200
 for details of manufacturers approved to this specification

1. Limiting conditions of use (contd)

1.5	Maximum power dissipation, per package	P_{D1}	200,0mW
	per output	P_{D2}	50,0mW
1.6	Maximum continuous current into any input.	$ I_I $	10,0mA
1.7	Maximum continuous current into any output.	$ I_O $	10,0mA
1.8	Operating temperature range	T_{amb}	
		Full	-55 to +125°C
		Limited	-40 to + 85°C
1.9	Storage temperature range	T_{stg}	-65 to +150°C
1.10	Transient energy rating		400V at 100pF through 1,5kΩ

1.11 Recommended handling precautions

- 1.11.1 Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method.
- 1.11.2 Use grounded tip soldering irons.
- 1.11.3 Ground all test equipment.
- 1.11.4 Connect all unused device inputs to V_{DD} or V_{SS} .
- 1.11.5 PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations.
- 1.11.6 Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices.
- 1.11.7 Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during inspection or handling.
- 1.11.8 When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage, 'Dummy connectors' should be used to electrically short all PC board terminals together.
- 1.11.9 Switch off power supply before inserting or removing devices from circuits.
- 1.11.10 Disconnect all low impedance equipment and input signals from the device before d.c. power supplies are switched off.

2. Recommended conditions of use and associated characteristics (not for inspection purposes)

These apply over the operating temperature range unless otherwise stated. All voltages referenced to V_{SS} .

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Quiescent device current	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range	Outputs open circuit	I_{DDA}	5,0	5,0	5,0	150,0	μA
		I_{DDA}	10,0	10,0	10,0	300,0	μA
		I_{DDA}	15,0	20,0	20,0	600,0	μA
Limited temperature range		I_{DDA}	5,0	20,0	20,0	150,0	μA
		I_{DDA}	10,0	40,0	40,0	300,0	μA
		I_{DDA}	15,0	80,0	80,0	600,0	μA
LOW level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OLA}	5,0	0,05	0,05	0,05	V
		V_{OLA}	10,0	0,05	0,05	0,05	V
		V_{OLA}	15,0	0,05	0,05	0,05	V
HIGH level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OHB}	5,0	4,95	4,95	4,95	V
		V_{OHB}	10,0	9,95	9,95	9,95	V
		V_{OHB}	15,0	14,95	14,95	14,95	V
LOW level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IL} = 1,5V$ $V_{IL} = 3,0V$ $V_{IL} = 4,0V$	V_{OLA}	5,0	0,5	0,5	0,5	V
		V_{OLA}	10,0	1,0	1,0	1,0	V
		V_{OLA}	15,0	1,5	1,5	1,5	V
HIGH level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IH} = 3,5V$ $V_{IH} = 7,0V$ $V_{IH} = 11,0V$	V_{OHB}	5,0	4,5	4,5	4,5	V
		V_{OHB}	10,0	9,0	9,0	9,0	V
		V_{OHB}	15,0	13,5	13,5	13,5	V
Output LOW (sink) current							
Full temperature range	$V_O = 0,4V$	I_{OLB}	5,0	0,64	0,51	0,36	mA
	$V_O = 0,5V$	I_{OLB}	10,0	1,60	1,30	0,90	mA
	$V_O = 1,5V$	I_{OLB}	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_O = 0,4V$	I_{OLB}	5,0	0,52	0,44	0,36	mA
	$V_O = 0,5V$	I_{OLB}	10,0	1,30	1,10	0,90	mA
	$V_O = 1,5V$	I_{OLB}	15,0	3,60	3,00	2,40	mA

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Output HIGH (source) current							
Full temperature range	$V_O = 4,6V$	$-I_{OHB}$	5,0	0,64	0,51	0,36	mA
	$V_O = 9,5V$	$-I_{OHB}$	10,0	1,60	1,30	0,90	mA
	$V_O = 13,5V$	$-I_{OHB}$	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_O = 4,6V$	$-I_{OHB}$	5,0	0,52	0,44	0,36	mA
	$V_O = 9,5V$	$-I_{OHB}$	10,0	1,30	1,10	0,90	mA
	$V_O = 13,5V$	$-I_{OHB}$	15,0	3,60	3,00	2,40	mA
Input leakage current	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range		$ I_{IA} $	15,0	0,10	0,10	1,00	μA
Limited temperature range		$ I_{IA} $	15,0	0,30	0,30	1,00	μA
Input capacitance per unit load (Any input)	$V_I = 0V$ $f = 1MHz$	C_{IA}	-	-	7,5	-	pF
Noise margin at LOW level output (equal to the difference between V_{IL} and V_{OL} for worst case combinations)		V_{NLB}	5,0	1,0	1,0	1,0	V
		V_{NLB}	10,0	2,0	2,0	2,0	V
		V_{NLB}	15,0	2,5	2,5	2,5	V
Noise margin at HIGH level output (equal to the difference between V_{IH} and V_{OH} for worst case combinations)		V_{NHB}	5,0	1,0	1,0	1,0	V
		V_{NHB}	10,0	2,0	2,0	2,0	V
		V_{NHB}	15,0	2,5	2,5	2,5	V
Propagation and Transition Times	$C_L = 50pF$ (Test conditions as in Sub-group A5)						

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25°C	T _{amb} HIGH	Unit
Transition Time LOW to HIGH level		t _{TLHA}	5,0	-	200,0	-	ns
		t _{TLHA}	10,0	-	100,0	-	ns
		t _{TLHA}	15,0	-	80,0	-	ns
		t _{THLA}	5,0	-	200,0	-	ns
		t _{THLA}	10,0	-	100,0	-	ns
		t _{THLA}	15,0	-	80,0	-	ns
Propagation Delay Time HIGH to LOW and LOW to HIGH level A or B to Q or $\bar{Q}$		t _{PLHA} / t _{PHLA}	5,0	-	600,0	-	ns
			10,0	-	300,0	-	ns
			15,0	-	220,0	-	ns
Propagation Delay Time HIGH to LOW and LOW to HIGH level C _D to Q or $\bar{Q}$		t _{PLHA} / t _{PHLA}	5,0	-	500,0	-	ns
			10,0	-	250,0	-	ns
			15,0	-	190,0	-	ns
HIGH or LOW Pulse Width		t _{PWHC}	5,0	-	70,0	-	ns
		t _{PWHC}	10,0	-	60,0	-	ns
		t _{PWHC}	15,0	-	50,0	-	ns
Retrigger Time		t _{rrB}	5,0	-	0,0	-	ns
		t _{rrB}	10,0	-	0,0	-	ns
		t _{rrB}	15,0	-	0,0	-	ns
Output Pulse Width Q or $\bar{Q}$ C _X = 0,002μF, R _X = 100KΩ C _X = 0,1μF, R _X = 100KΩ C _X = 10,0μF, R _X = 100KΩ		t _{PWZL}	5,0	-	210,0	-	μs
		t _{PWZL}	10,0	-	212,0	-	μs
		t _{PWZL}	15,0	-	214,0	-	μs
		t _{PWZL}	5,0	-	9,3	-	ms
		t _{PWZL}	10,0	-	9,5	-	ms
		t _{PWZL}	15,0	-	9,6	-	ms
		t _{PWZL}	5,0	-	0,915	-	s
		t _{PWZL}	10,0	-	0,93	-	s
		t _{PWZL}	15,0	-	0,94	-	s
		t _{PWZL}	5,0	-	0,915	-	s
		t _{PWZL}	10,0	-	0,93	-	s
		t _{PWZL}	15,0	-	0,94	-	s

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25°C	T _{amb} HIGH	Unit
Pulse Width Match between circuits in the same package C _X = 0,1pF, R _X = 1000KΩ		$\frac{100 (T1 - T2)}{T1}$	5,0	-	±1,0	-	% Typ.
			10,0	-	±1,0	-	% Typ.
			15,0	-	±1,0	-	% Typ.
External Timing Resistance		R _{XB}		-	5,0	-	KΩ
		R _{XA}		-	*	-	KΩ
External Timing Capacitance		C _{XB}		-	0,0	-	pF
		C _{XA}		-	No Limit	-	pF

*The maximum usable resistance R_X is a function of the leakage of capacitance C_X, the leakage of the device, and the leakage due to board layout and surface resistance.

Terminal identification

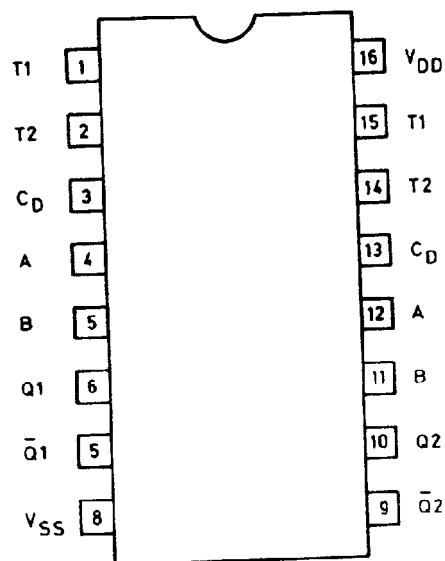
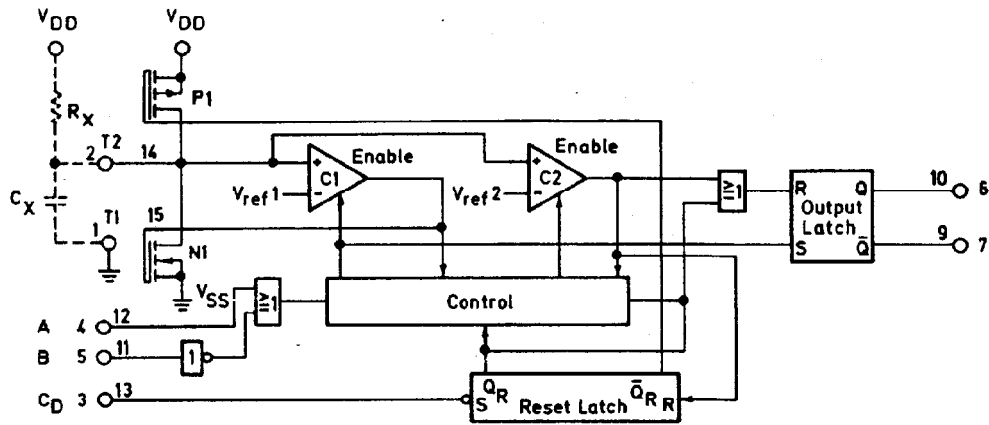


Figure 1

Typical logic diagram



(This is a graphic representation, not a circuit diagram

Figure 2

Switching time waveforms

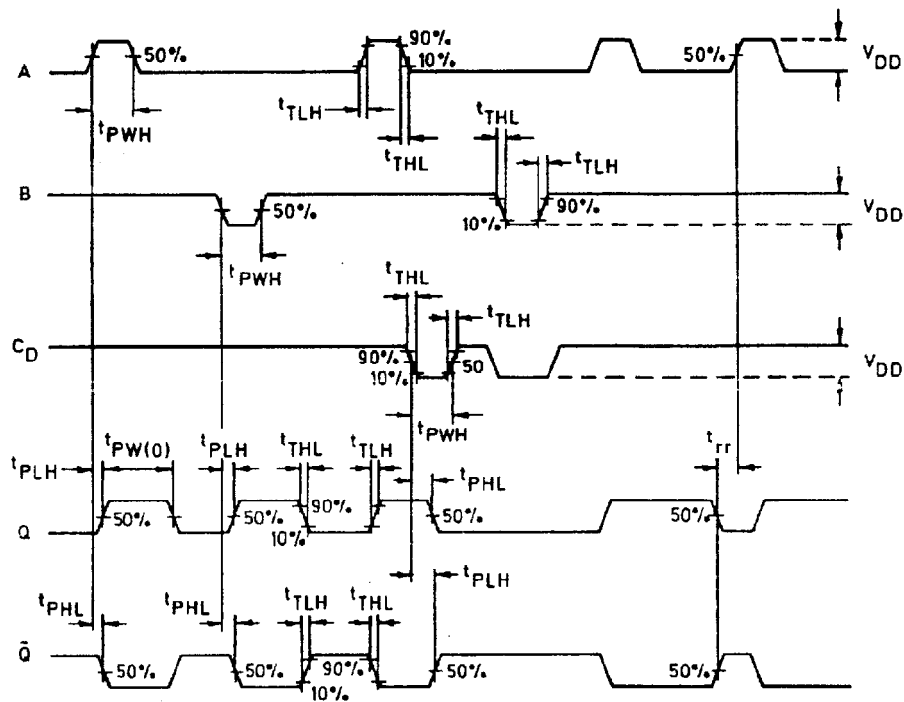


Figure 3

Timing diagram

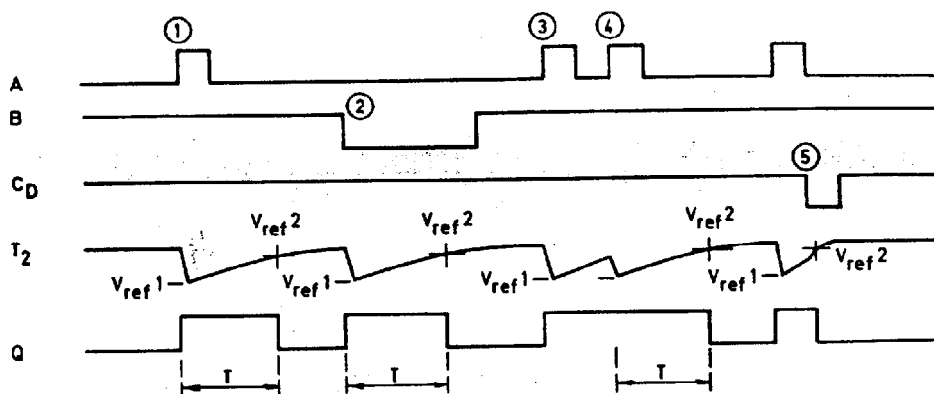


Figure 4

Theory of operation

Trigger operation

As shown in Figure 4, before an input trigger occurs, the monostable is in the quiescent state with the Q output LOW, and the timing capacitor C_x completely charged to V_{DD} . When the trigger input A goes from V_{SS} to V_{DD} (while inputs B and C_D are held to V_{DD}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1 ①. At the same time the output latch is set. With transistor N1 on, the capacitor C_x rapidly discharges toward V_{SS} until $V_{ref 1}$ is reached. At this point the output of comparator C1 changes level and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_x begins to charge through the timing resistor, R_x , toward V_{DD} . When the voltage across C_x equals $V_{ref 2}$, comparator C2 changes level, causing the output latch to reset (Q goes LOW) while at the same time disabling comparator C2 ②. This ends the timing cycle with the monostable in the quiescent state waiting for the next trigger.

It should be noted that in the quiescent state C_x is fully charged to V_{DD} causing the current through resistor R_x to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. The output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_x , R_x , or the duty cycle of the input waveform.

Retrigger operation

The 4538B is retriggered if a valid trigger occurs ③ followed by another valid trigger ④ before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from $V_{ref 1}$, but has not yet reached $V_{ref 2}$, will cause an increase in output pulse width T. When a valid retrigger is initiated ④, the voltage at T2 will again drop to $V_{ref 1}$ before progressing along the RC charging curve toward V_{DD} . The Q output will remain HIGH until time T, after the last valid retrigger.