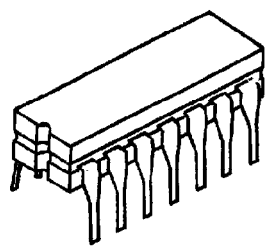


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90 104 - 180 ISSUE 1 DECEMBER 1981 Page 1 of 25 pages
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	 MANUFACTURERS TYPE NUMBER 4541B SEE PD 9002 AND CECC 00 200 For ordering information see page 11
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1976 BS CECC 90 100 : 1977	PROGRAMMABLE OSCILLATOR/ TIMER SILICON COMPLEMENTARY MOS. WITH (B) BUFFERED OUTPUTS AND CAVITY PACKAGING.
Outline not to scale: Isometric projection Marking information see page 10  For detail dimensions see IEC 191-2 (A50B)	Assessment levels R, S, T and V and optional screening categories A, B, C and D

CAUTION: THESE ARE STATIC SENSITIVE DEVICES - See clause 1.11

1. Limiting conditions of use (not for inspection purposes)

All voltages referenced to V_{SS}

1.1	Maximum supply voltage, positive	V_{DD}	+18,0V
1.2	Maximum supply voltage, negative	V_{DD}	-0,5V
1.3	Maximum positive input voltage	V_I V_{DD}	+0,5V
1.4	Maximum negative input voltage	V_I	-0,5V

Refer to Qualified Products List PD 9002 and/or CECC 00 200
 for details of manufacturers approved to this specification

1. Limiting conditions of use (contd)

1.5	Maximum power dissipation, per package	P_{D1}	200,0mW
	per output	P_{D2}	200,0mW
1.6	Maximum continuous current into any input.	$ I_I $	10,0mA
1.7	Maximum continuous current into any output.	$ I_O $	10,0mA
1.8	Operating temperature range	T_{amb}	
		Full	-55 to +125°C
		Limited	-40 to + 85°C
1.9	Storage temperature range	T_{stg}	-65 to +150°C
1.10	Transient energy rating		400V at 100pF through 1,5kΩ
1.11	<u>Recommended handling precautions</u>		
1.11.1	Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method.		
1.11.2	Use grounded tip soldering irons.		
1.11.3	Ground all test equipment.		
1.11.4	Connect all unused device inputs to V_{DD} or V_{SS} .		
1.11.5	PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations.		
1.11.6	Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices.		
1.11.7	Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during inspection or handling.		
1.11.8	When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage, 'Dummy connectors' should be used to electrically short all PC board terminals together.		
1.11.9	Switch off power supply before inserting or removing devices from circuits.		
1.11.10	Disconnect all low impedance equipment and input signals from the device before d.c. power supplies are switched off.		

2. Recommended conditions of use and associated characteristics (not for inspection purposes)

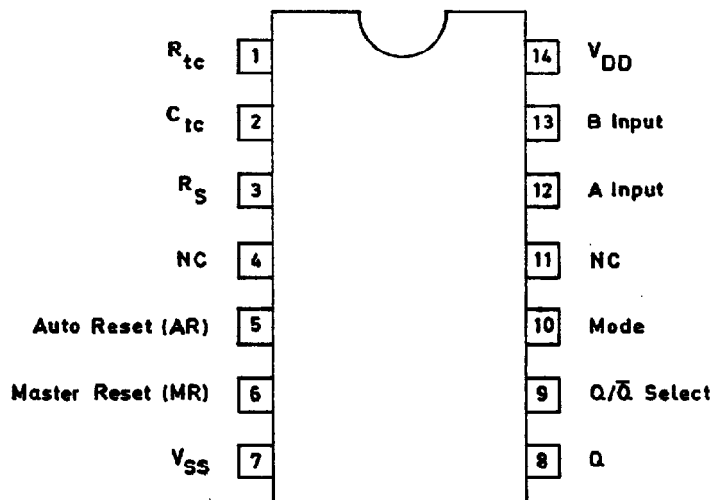
These apply over the operating temperature range unless otherwise stated. All voltages referenced to V_{SS} .

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Quiescent device current	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range	Outputs open circuit	I_{DDA}	5,0	5,0	5,0	150,0	μA
		I_{DDA}	10,0	10,0	10,0	300,0	μA
		I_{DDA}	15,0	20,0	20,0	600,0	μA
Limited temperature range		I_{DDA}	5,0	20,0	20,0	150,0	μA
		I_{DDA}	10,0	40,0	40,0	300,0	μA
		I_{DDA}	15,0	80,0	80,0	600,0	μA
Auto Reset Quiescent current	(Pin 5 is LOW)	I_{DDRA}	5,0	200,0	200,0	1200,0	μA
		I_{DDRA}	10,0	250,0	250,0	1500,0	μA
		I_{DDRA}	15,0	500,0	500,0	2000,0	μA
LOW level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OLA}	5,0	0,05	0,05	0,05	V
		V_{OLA}	10,0	0,05	0,05	0,05	V
		V_{OLA}	15,0	0,05	0,05	0,05	V
HIGH level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OHB}	5,0	4,95	4,95	4,95	V
		V_{OHB}	10,0	9,95	9,95	9,95	V
		V_{OHB}	15,0	14,95	14,95	14,95	V
LOW level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IL} = 1,5V$ $V_{IL} = 3,0V$ $V_{IL} = 4,0V$	V_{OLA}	5,0	0,5	0,5	0,5	V
		V_{OLA}	10,0	1,0	1,0	1,0	V
		V_{OLA}	15,0	1,5	1,5	1,5	V
HIGH level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IH} = 3,5V$ $V_{IH} = 7,0V$ $V_{IH} = 11,0V$	V_{OHB}	5,0	4,5	4,5	4,5	V
		V_{OHB}	10,0	9,0	9,0	9,0	V
		V_{OHB}	15,0	13,5	13,5	13,5	V
Output LOW (sink) current							
Full temperature range	$V_O = 0,4V$ $V_O = 0,5V$ $V_O = 1,5V$	I_{OLB}	5,0	0,64	0,51	0,36	mA
		I_{OLB}	10,0	1,60	1,30	0,90	mA
		I_{OLB}	15,0	4,20	3,40	2,40	mA

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25°C	T _{amb} HIGH	Unit
Output LOW (sink) current (contd)							
Limited temperature range	V _O = 0,4V	I _{OLB}	5,0	0,52	0,44	0,36	mA
	V _O = 0,5V	I _{OLB}	10,0	1,30	1,10	0,90	mA
	V _O = 1,5V	I _{OLB}	15,0	3,60	3,00	2,40	mA
Output HIGH (source) current							
Full temperature range	V _O = 4,6V	-I _{OHB}	5,0	7,96	6,42	4,49	mA
	V _O = 9,5V	-I _{OHB}	10,0	4,19	3,38	2,37	mA
	V _O = 13,5V	-I _{OHB}	15,0	16,3	13,2	9,24	mA
Limited temperature range	V _O = 4,6V	-I _{OHB}	5,0	5,1	4,27	3,5	mA
	V _O = 9,5V	-I _{OHB}	10,0	2,69	2,25	1,85	mA
	V _O = 13,5V	-I _{OHB}	15,0	10,5	8,8	7,22	mA
Input leakage current	V _{IL} = 0V V _{IH} = V _{DD}						
Full temperature range		I _{IA}	15,0	0,10	0,10	1,00	μA
Limited temperature range		I _{IA}	15,0	0,30	0,30	1,00	μA
Input capacitance per unit load (Any input)	V _I = 0V f = 1MHz	C _{IA}	-	-	7,5	-	pF
Noise margin at LOW level output (equal to the difference between V _{IL} and V _{OL} for worst case combinations)		V _{NLB} V _{NLB} V _{NLB}	5,0 10,0 15,0	1,0 2,0 2,5	1,0 2,0 2,5	1,0 2,0 2,5	V V V
Noise margin at HIGH level output (equal to the difference between V _{IH} and V _{OH} for worst case combinations)		V _{NHB} V _{NHB} V _{NHB}	5,0 10,0 15,0	1,0 2,0 2,5	1,0 2,0 2,5	1,0 2,0 2,5	V V V
Propagation and Transition Times	C _L = 50pF (Test conditions as in Sub-group A5)						

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25°C	T _{amb} HIGH	Unit
Transition Time HIGH to LOW level		t _{TLHA}	5,0	-	360,0	-	ns
		t _{TLHA}	10,0	-	180,0	-	ns
		t _{TLHA}	15,0	-	130,0	-	ns
		t _{THLA}	5,0	-	200,0	-	ns
		t _{THLA}	10,0	-	100,0	-	ns
		t _{THLA}	15,0	-	80,0	-	ns
Propagation Delay Time HIGH to LOW and LOW to HIGH level Clock to Q (Output = 2 ⁸)		t _{PHLA} /	5,0	-	10,5	-	μs
		t _{PLHA}	10,0	-	3,8	-	μs
		t _{PLHA}	15,0	-	2,9	-	μs
Propagation Delay Time HIGH to LOW and LOW to HIGH level Clock to Q (Output = 2 ¹⁶)		t _{PHLA} /	5,0	-	18,0	-	μs
		t _{PLHA}	10,0	-	10,0	-	μs
		t _{PLHA}	15,0	-	7,5	-	μs
Clock Pulse Width		t _{PWCB}	5,0	-	900,0	-	ns
		t _{PWCB}	10,0	-	300,0	-	ns
		t _{PWCB}	15,0	-	225,0	-	ns
Clock Pulse Frequency		Freq.A	5,0	-	1,0	-	MHz
		Freq.A	10,0	-	3,0	-	MHz
		Freq.A	15,0	-	4,0	-	MHz
Master Reset Pulse Width		t _{PWRB}	5,0	-	900,0	-	ns
		t _{PWRB}	10,0	-	300,0	-	ns
		t _{PWRB}	15,0	-	225,0	-	ns

Terminal identification



Terminals marked with NC are not connected internally and may be used as electrical support points.

Figure 1

Function table

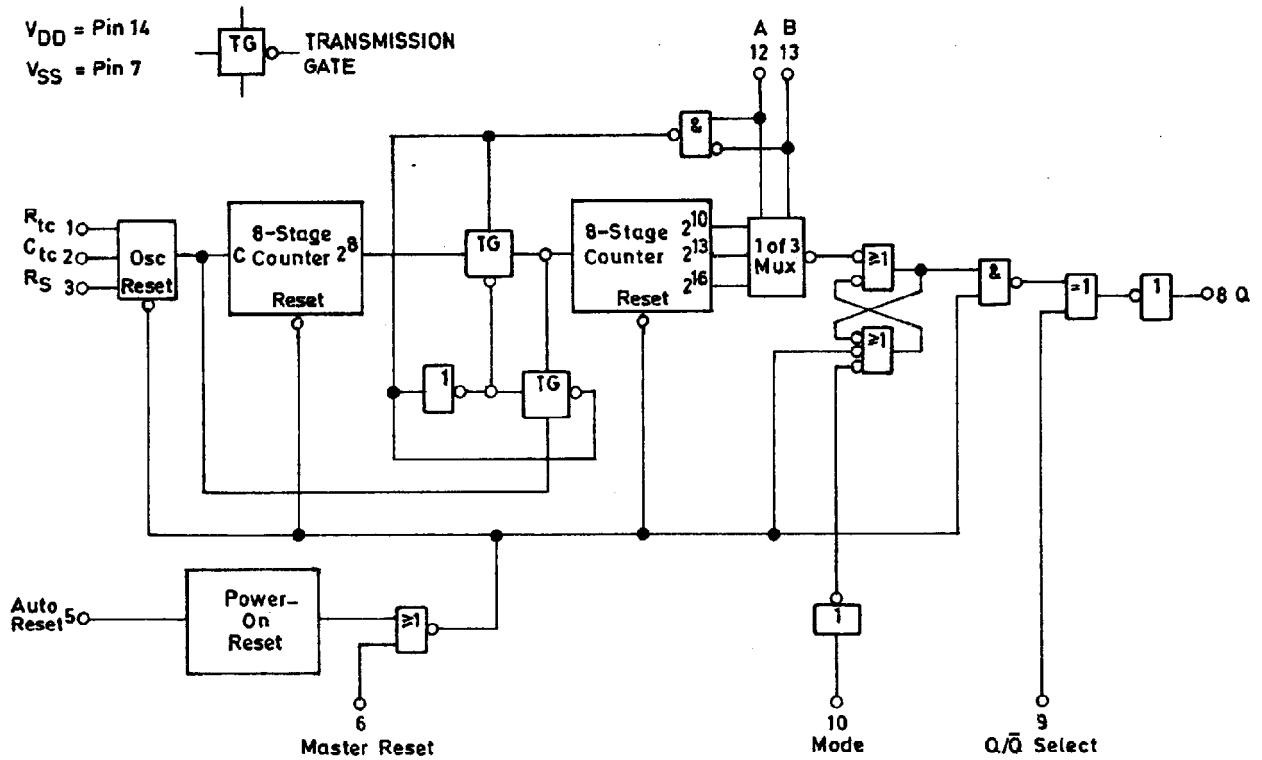
PIN	LEVEL	
	LOW	HIGH
5	Auto Reset Operating	Auto Reset Disabled
6	Timer Operational	Master Reset On
9	Output Initially LOW After Reset	Output Initially HIGH After Reset
10	Single Cycle Mode	Recycle Mode

Frequency selection table

A	B	NUMBER OF COUNTER STAGES n	COUNT 2^n
L	L	13	8192
L	H	10	1024
H	L	8	256
H	H	16	65536

H = HIGH level
L = LOW level

Typical logic diagram



This is a graphic representation, not a circuit diagram.

Figure 2

Switching time waveforms

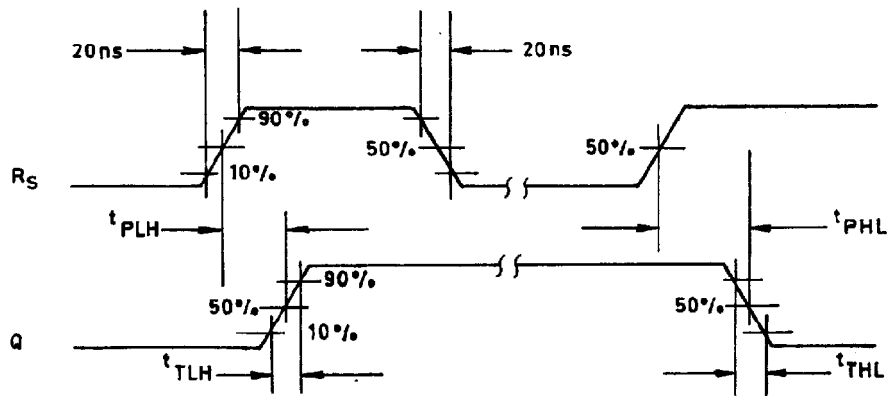


Figure 3

General

Operating Characteristics

With Auto Reset pin set to a LOW the counter circuit is initialized by turning on the power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a HIGH. Both types of reset will result in synchronously resetting all counter stages independent of counter state. The Auto Reset pin when set to a HIGH provides the low power operation.

The RC oscillator as shown in Figure 4 will oscillate with a frequency determined by the external RC network i.e.,

$$f = \frac{1}{2.3 R_{tc} C_{tc}} \quad \text{if } (1,0\text{kHz} \leq f \leq 100,0\text{kHz})$$

and $R_S \geq 2 R_{tc}$ where $R_S \geq 10,0\text{k}\Omega$

The time select inputs (A and B) provide a two-bit address to output any one of four counter stages (2^8 , 2^{10} , 2^{13} and 2^{16}). The 2^n counts as shown in the Frequency Selection Table (Table 2) represents the Q output of the N^{th} stage of the counter. When A is HIGH, 2^{16} is selected for both states of B. However, when B is LOW, normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputting 2^8).

The $Q/\bar{Q}$ select output control pin provides for a choice of output level. When the counter is in a reset condition and $Q/\bar{Q}$ select pin is set to a LOW the Q output is a LOW correspondingly when $Q/\bar{Q}$ select pin is set to a HIGH the Q output is a HIGH.

When the mode control pin is set to a HIGH the selected count is continually transmitted to the output. But, with mode pin LOW and after a reset condition the RS bistable (see Figure 2) resets, counting commences and after 2^{n-1} counts the RS bistable sets which causes the output to change state. Hence, after another 2^{n-1} counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

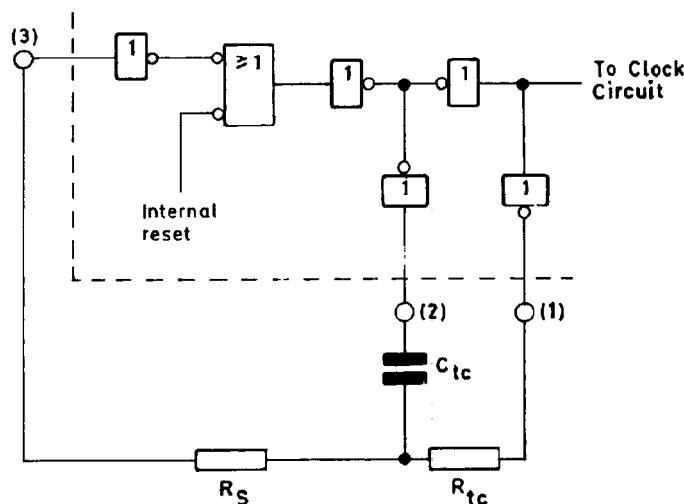


Figure 4