

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 AND

BS CECC 90 104 - 186

ISSUE 1

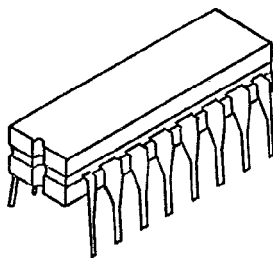
DECEMBER 1981



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ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:BS CECC 90 000 : 1976
BS CECC 90 100 : 1977

MANUFACTURERS TYPE NUMBER

4043BSEE PD 9002 AND CECC 00 200
For ordering information
see page 10Outline not to scale: Isometric projection
Marking information see page 9QUAD NOR R-S LATCH WITH
3 STATE OUTPUTSSILICON COMPLEMENTARY MOS.
WITH (B) BUFFERED OUTPUTS AND
CAVITY PACKAGING.Assessment levels
R, S, T and V
and optional screening
categories A, B, C and D

For detail dimensions see IEC 191-2 (A50C)

CAUTION: THESE ARE STATIC SENSITIVE DEVICES - See clause 1.11Limiting conditions of use (not for inspection purposes)All voltages referenced to V_{SS}

- 1.1 Maximum supply voltage, positive
- 1.2 Maximum supply voltage, negative
- 1.3 Maximum positive input voltage
- 1.4 Maximum negative input voltage

V_{DD}	+18,0V
V_{DD}	-0,5V
V_I	V_{DD} +0,5V
V_I	-0,5V

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1. Limiting conditions of use (contd)

1.5	Maximum power dissipation, per package per output	P_{D1} P_{D2}	200,0mW 50,0mW
1.6	Maximum continuous current into any input.	$ I_I $	10,0mA
1.7	Maximum continuous current into any output.	$ I_O $	10,0mA
1.8	Operating temperature range	T_{amb} Full Limited	-55 to +125°C -40 to + 85°C
1.9	Storage temperature range	T_{stg}	-65 to +150°C
1.10	Transient energy rating		400V at 100pF through 1,5kΩ
1.11	<u>Recommended handling precautions</u>		
1.11.1	Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method.		
1.11.2	Use grounded tip soldering irons.		
1.11.3	Ground all test equipment.		
1.11.4	Connect all unused device inputs to V_{DD} or V_{SS} .		
1.11.5	PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations.		
1.11.6	Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices.		
1.11.7	Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during inspection or handling.		
1.11.8	When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage, 'Dummy connectors' should be used to electrically short all PC board terminals together.		
1.11.9	Switch off power supply before inserting or removing devices from circuits.		
1.11.10	Disconnect all low impedance equipment and input signals from the device before d.c. power supplies are switched off.		

2. Recommended conditions of use and associated characteristics (not for inspection purposes)

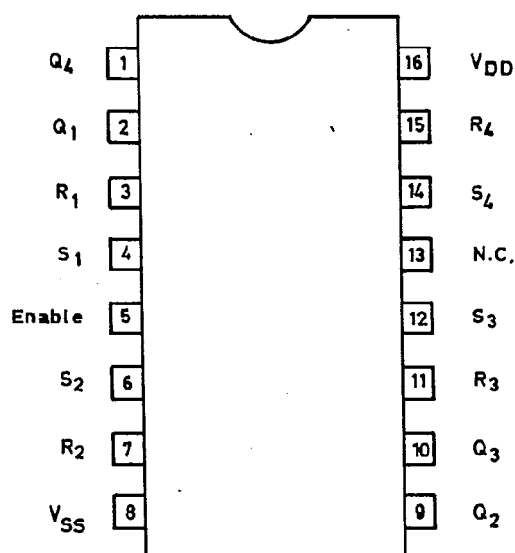
These apply over the operating temperature range unless otherwise stated. All voltages referenced to V_{SS} .

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Quiescent device current	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range	Outputs open circuit	I_{DDA}	5,0	1,0	1,0	30,0	μA
		I_{DDA}	10,0	2,0	2,0	60,0	μA
		I_{DDA}	15,0	4,0	4,0	120,0	μA
Limited temperature range		I_{DDA}	5,0	4,0	4,0	30,0	μA
		I_{DDA}	10,0	8,0	8,0	60,0	μA
		I_{DDA}	15,0	16,0	16,0	120,0	μA
LOW level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OLA}	5,0	0,05	0,05	0,05	V
		V_{OLA}	10,0	0,05	0,05	0,05	V
		V_{OLA}	15,0	0,05	0,05	0,05	V
HIGH level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OHB}	5,0	4,95	4,95	4,95	V
		V_{OHB}	10,0	9,95	9,95	9,95	V
		V_{OHB}	15,0	14,95	14,95	14,95	V
LOW level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IL} = 1,5V$ $V_{IL} = 3,0V$ $V_{IL} = 4,0V$	V_{OLA}	5,0	0,5	0,5	0,5	V
		V_{OLA}	10,0	1,0	1,0	1,0	V
		V_{OLA}	15,0	1,5	1,5	1,5	V
HIGH level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IH} = 3,5V$ $V_{IH} = 7,0V$ $V_{IH} = 11,0V$	V_{OHB}	5,0	4,5	4,5	4,5	V
		V_{OHB}	10,0	9,0	9,0	9,0	V
		V_{OHB}	15,0	13,5	13,5	13,5	V
Output LOW (sink) current							
Full temperature range	$V_O = 0,4V$ $V_O = 0,5V$ $V_O = 1,5V$	I_{OLB}	5,0	0,64	0,51	0,36	mA
		I_{OLB}	10,0	1,60	1,30	0,90	mA
		I_{OLB}	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_O = 0,4V$ $V_O = 0,5V$ $V_O = 1,5V$	I_{OLB}	5,0	0,52	0,44	0,36	mA
		I_{OLB}	10,0	1,30	1,10	0,90	mA
		I_{OLB}	15,0	3,60	3,00	2,40	mA

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Output HIGH (source) current							
Full temperature range	$V_O = 4,6V$	$-I_{OHB}$	5,0	0,25	0,2	0,14	mA
	$V_O = 9,5V$	$-I_{OHB}$	10,0	0,62	0,5	0,35	mA
	$V_O = 13,5V$	$-I_{OHB}$	15,0	1,80	1,5	1,10	mA
Limited temperature range	$V_O = 4,6V$	$-I_{OHB}$	5,0	0,2	0,16	0,12	mA
	$V_O = 9,5V$	$-I_{OHB}$	10,0	0,5	0,40	0,30	mA
	$V_O = 13,5V$	$-I_{OHB}$	15,0	1,4	1,20	1,00	mA
Input leakage current	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range		$ I_{IA} $	15,0	0,10	0,10	1,00	μA
Limited temperature range		$ I_{IA} $	15,0	0,30	0,30	1,00	μA
Three state output leakage current (combined to obtain a high impedance output state)	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range		$ I_{OZA} $	15,0	0,1	0,1	3,0	μA
Limited temperature range		$ I_{OZA} $	15,0	1,0	1,0	7,5	μA
Input capacitance per unit load (Any input)	$V_I = 0V$ $f = 1MHz$	C_{IA}	-	-	7,5	-	pF
Noise margin at LOW level output (equal to the difference between V_{IL} and V_{OL} for worst case combinations)		V_{NLB}	5,0	1,0	1,0	1,0	V
		V_{NLB}	10,0	2,0	2,0	2,0	V
		V_{NLB}	15,0	2,5	2,5	2,5	V
Noise margin at HIGH level output (equal to the difference between V_{IH} and V_{OH} for worst case combinations)		V_{NHB}	5,0	1,0	1,0	1,0	V
		V_{NHB}	10,0	2,0	2,0	2,0	V
		V_{NHB}	15,0	2,5	2,5	2,5	V

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Propagation and transition times	$C_L = 50pF$ (Test conditions as in sub-group A5)						
Propagation Delay Time		$t_{PHLA}/$	5,0	-	350,0	-	ns
HIGH to LOW and LOW to HIGH level		t_{PLHA}	10,0	-	175,0	-	ns
Set or Reset			15,0	-	120,0	-	ns
Transition Time		$t_{THLA}/$	5,0	-	200,0	-	ns
HIGH to LOW and LOW to HIGH level		t_{TLHA}	10,0	-	100,0	-	ns
Set or Reset			15,0	-	80,0	-	ns
Pulse Width		$t_{PWRB}/$	5,0	-	200,0	-	ns
Set or Reset		t_{PWSB}	10,0	-	100,0	-	ns
			15,0	-	70,0	-	ns
Three State Propagation Delay Time		$t_{PLZA}/$	5,0	-	300,0	-	ns
Enable to Outputs		t_{PZLA}	10,0	-	160,0	-	ns
		$t_{PHZA}/$	15,0	-	110,0	-	ns
		t_{PZHA}					

Terminal identification



Terminals marked NC are not connected internally and may be used as electrical support points.

Figure 1

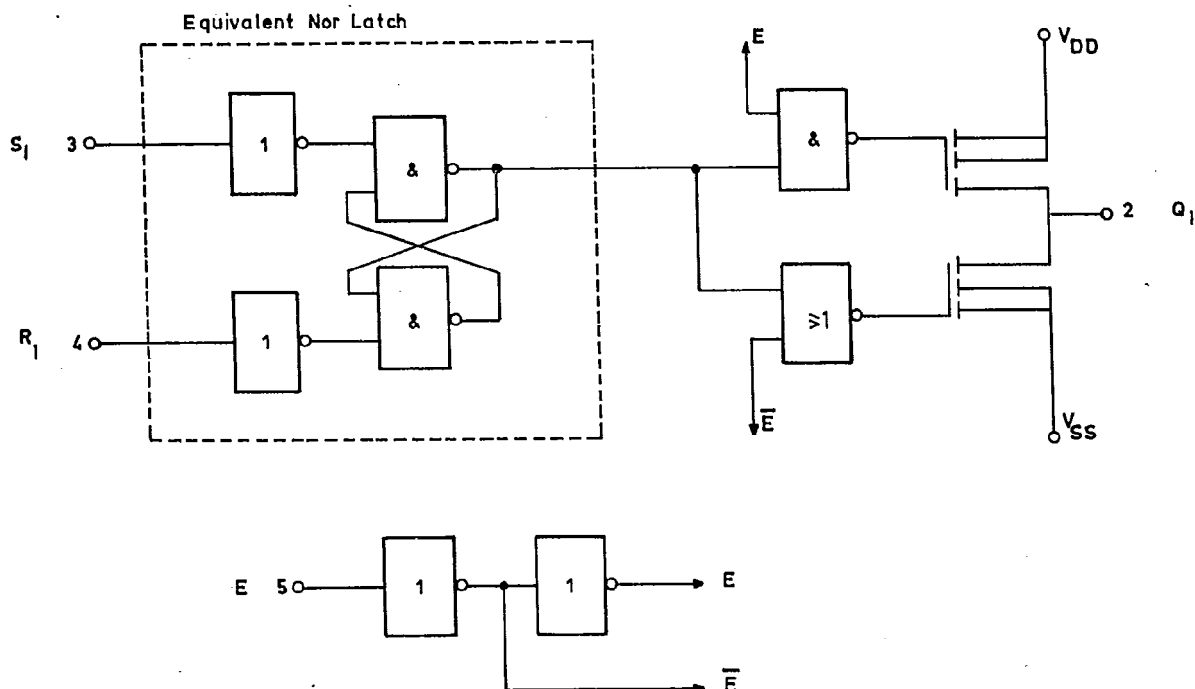
Function table

Table 1

INPUTS			OUTPUTS
R	S	E	Q
X	X	L	High Impedance
L	L	H	L
L	H	H	H
H	L	H	L
H	H	H	No Change

H = HIGH level
L = LOW level
X = Level irrelevant

Typical logic diagram



V_{SS} = Pin 8

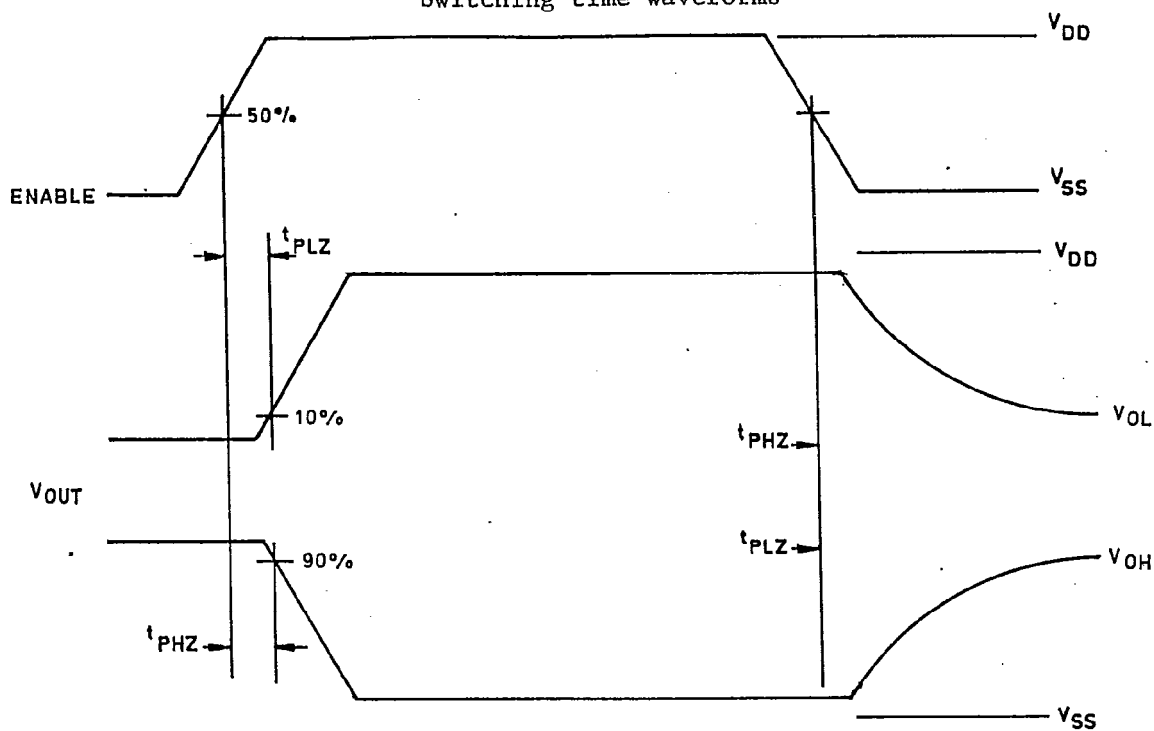
V_{DD} = Pin 16

(ONE QUARTER OF DEVICE SHOWN)

This is a graphic representation, not a circuit diagram

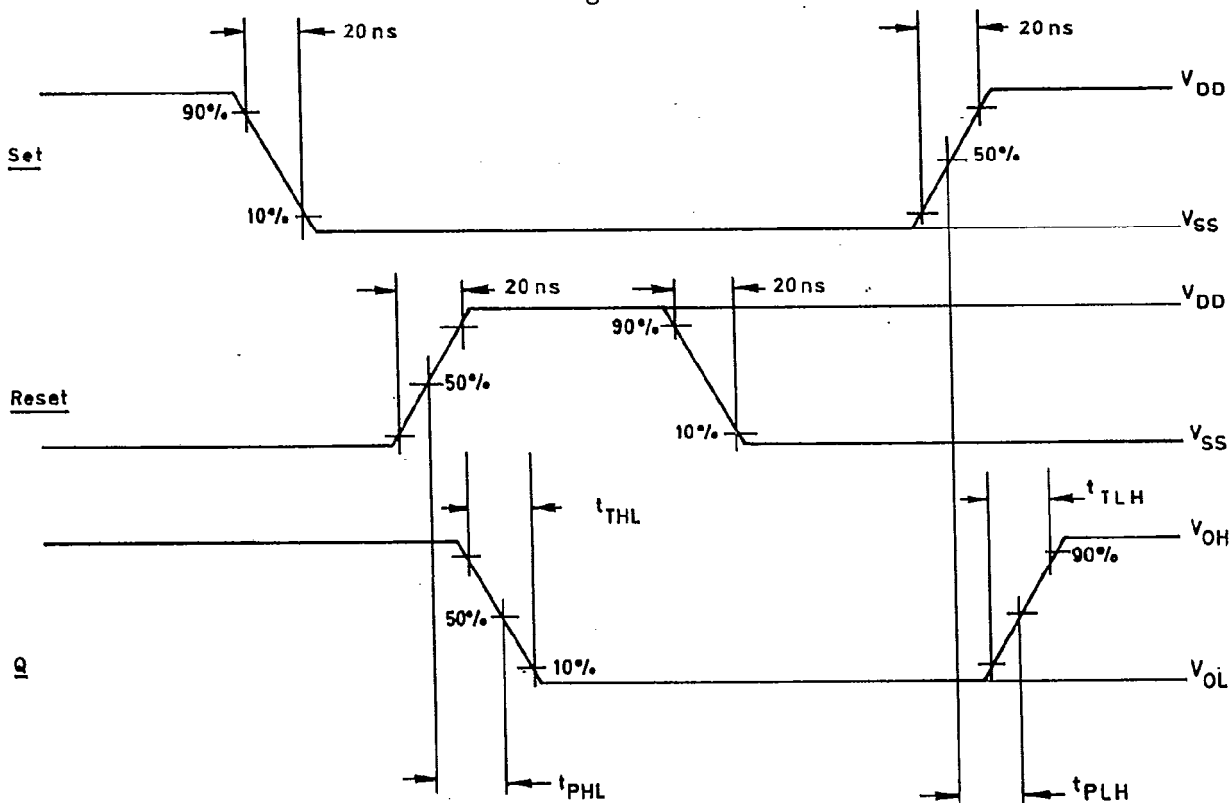
Figure 2

Switching time waveforms



Pins 4,6,12,14 = V_{DD} Pins 3,7,11,15 = V_{DD}
 V_{Out2} = Pins 3,7,11,15 = V_{SS} V_{Out1} = Pins 4,1,12,14 = V_{SS}
 Pins 2,9,10,1 to V_{SS} via $1K\Omega$ Pins 2,9,10,1 to V_{DD} via $1K\Omega$

Three state propagation delay times
 Figure 3



Set, Reset propagation delay times
 Figure 4

Marking

The following shall be marked on the device, in the following order of precedence, as space permits. All information, except the terminal marking shall appear on the primary package used as initial protection or wrapping for delivery:

- (1) Terminal identification
- (2) Type number
- (3) Operating temperature range (if not included in 2)
- (4) Quality assessment level applied
- (5) Screening class applied
- (6) Date-code (year-week defined by three or four figures)
- (7) Mark of conformity (CECC logo)
- (8) Manufacturers name or trade mark (may include factory code)
- (9) Factory identification code
- (10) Package materials
- (11) Caution label for devices susceptible to damage by electrostatic discharge
- (12) Optional tests

The marking symbols shall be located following the figures below.

The underside of the package is free for manufacturers additional marking

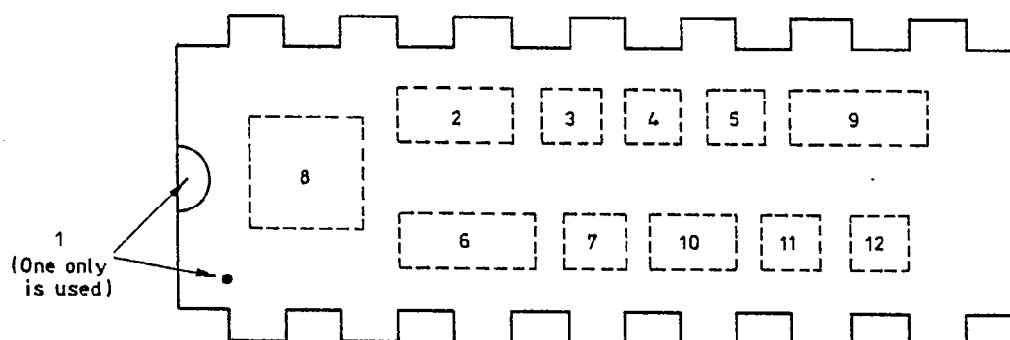


Figure 5