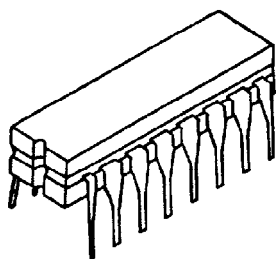


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON. W1A 2BS	BS CECC 90 104 - 201 ISSUE 1 FEBRUARY 1982  Page 1 of 30 pages
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND	MANUFACTURERS TYPE NUMBER 4568B SEE PD 9002 AND CECC 00 200 For ordering information see page 14
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC-90 000 : 1976 BS CECC 90 100 : 1977	PHASE COMPARATOR AND TWO PROGRAMMABLE COUNTERS WITH THREE STATE OUTPUTS
Outline not to scale: Isometric projection Marking information see page 13  For detail dimensions see IEC 191-2 (A50C)	SILICON COMPLEMENTARY MOS. WITH (B) BUFFERED OUTPUTS AND CAVITY PACKAGING.
	Assessment levels R, S, T and V and optional screening categories A, B, C and D

CAUTION: THESE ARE STATIC SENSITIVE DEVICES - See clause 1.11

Limiting conditions of use (not for inspection purposes)

All voltages referenced to V_{SS}

1.1	Maximum supply voltage, positive	V_{DD}	+18,0V
1.2	Maximum supply voltage, negative	V_{DD}	-0,5V
1.3	Maximum positive input voltage	V_I	V_{DD} +0,5V
1.4	Maximum negative input voltage	V_I	-0,5V

Refer to Qualified Products List PD 9002 and/or CECC 00 200
 for details of manufacturers approved to this specification

- | | | | |
|---------|--|-----------|-----------------------------|
| 1 | <u>Limiting conditions of use</u> (contd) | | |
| 1.5 | Maximum power dissipation, per package | P_{D1} | 200,0mW |
| | per output | P_{D2} | 50,0mA |
| 1.6 | Maximum continuous current into any input. | $ I_I $ | 10,0mA |
| 1.7 | Maximum continuous current into any output. | $ I_O $ | 10,0mA |
| 1.8 | Operating temperature range | T_{amb} | |
| | | Full | -55 to +125°C |
| | | Limited | -40 to + 85°C |
| 1.9 | Storage temperature range | T_{stg} | -65 to 150°C |
| 1.10 | Transient energy rating | | 400V at 100pF through 1,5kΩ |
| 1.11 | <u>Recommended handling precautions</u> | | |
| 1.11.1 | Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method. | | |
| 1.11.2 | Use grounded tip soldering irons. | | |
| 1.11.3 | Ground all test equipment. | | |
| 1.11.4 | Connect all unused device inputs to V_{DD} or V_{SS} . | | |
| 1.11.5 | PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations. | | |
| 1.11.6 | Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices. | | |
| 1.11.7 | Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding technique during inspection or handling. | | |
| 1.11.8 | When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage, 'Dummy connectors' should be used to electrically short all PC board terminals together. | | |
| 1.11.9 | Switch off power supply before inserting or removing devices from circuits. | | |
| 1.11.10 | Disconnect all low impedance equipment and input signals from the device before d.c. power supplies are switched off. | | |

2. Recommended conditions of use and associated characteristics (not for inspection purposes)

These apply over the operating temperature range unless otherwise stated. All voltages referenced to V_{SS} .

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Quiescent device current	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range	Outputs open circuit	I_{DDA}	5,0	5,0	5,0	150,0	μA
		I_{DDA}	10,0	10,0	10,0	300,0	μA
		I_{DDA}	15,0	20,0	20,0	600,0	μA
Limited temperature range		I_{DDA}	5,0	20,0	20,0	150,0	μA
		I_{DDA}	10,0	40,0	40,0	300,0	μA
		I_{DDA}	15,0	80,0	80,0	600,0	μA
LOW level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OLA}	5,0	0,05	0,05	0,05	V
		V_{OLA}	10,0	0,05	0,05	0,05	V
		V_{OLA}	15,0	0,05	0,05	0,05	V
HIGH level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OHB}	5,0	4,95	4,95	4,95	V
		V_{OHB}	10,0	9,95	9,95	9,95	V
		V_{OHB}	15,0	14,95	14,95	14,95	V
LOW level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IL} = 1,5V$ $V_{IL} = 3,0V$ $V_{IL} = 4,0V$	V_{OLA}	5,0	0,5	0,5	0,5	V
		V_{OLA}	10,0	1,0	1,0	1,0	V
		V_{OLA}	15,0	1,5	1,5	1,5	V
HIGH level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IH} = 3,5V$ $V_{IH} = 7,0V$ $V_{IH} = 11,0V$	V_{OHB}	5,0	4,5	4,5	4,5	V
		V_{OHB}	10,0	9,0	9,0	9,0	V
		V_{OHB}	15,0	13,5	13,5	13,5	V
Output LOW (sink) current							
Full temperature range	$V_O = 0,4V$	I_{OLB}	5,0	0,64	0,51	0,36	mA
	$V_O = 0,5V$	I_{OLB}	10,0	1,60	1,30	0,90	mA
	$V_O = 1,5V$	I_{OLB}	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_O = 0,4V$	I_{OLB}	5,0	0,52	0,44	0,36	mA
	$V_O = 0,5V$	I_{OLB}	10,0	1,30	1,10	0,90	mA
	$V_O = 1,5V$	I_{OLB}	15,0	3,60	3,00	2,40	mA

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25°C	T _{amb} HIGH	Unit
Output HIGH (source) current							
Full temperature range	V _O = 4,6V	-I _{OHB}	5,0	0,20	0,20	0,14	mA
	V _O = 9,5V	-I _{OHB}	10,0	0,62	0,50	0,35	mA
	V _O = 13,5V	-I _{OHB}	15,0	1,80	1,50	1,10	mA
Limited temperature range	V _O = 4,6V	-I _{OHB}	5,0	0,20	0,16	0,12	mA
	V _O = 9,5V	-I _{OHB}	10,0	0,50	0,40	0,30	mA
	V _O = 13,5V	-I _{OHB}	15,0	1,40	1,20	1,00	mA
Input leakage current	V _{IL} = 0V V _{IH} = V _{DD}						
Full temperature range		I _{IA}	15,0	0,10	0,10	1,00	μA
Limited temperature range		I _{IA}	15,0	0,30	0,30	1,00	μA
Three state output leakage current (combined to obtain high impedance output state)	V _{DisA} = V _{DD}						
Full temperature range		I _{OZA}	15,0	±0,1	±0,1	±3,0	μA
Limited temperature range		I _{OZA}	15,0	±1,0	±1,0	±7,5	μA
Phase comparator input resistance (Typical values)		R _{IN}	5,0	-	10 ⁶	-	MΩ
		R _{IN}	10,0	-	10 ⁶	-	MΩ
		R _{IN}	15,0	-	10 ⁶	-	MΩ
Input capacitance per unit load (Any input)	V _I = 0V f = 1MHz	C _{IA}	-	-	7,5	-	pF
Noise margin at LOW level output (equal to the difference between V _{IL} and V _{OL} for worst case combinations)		V _{NLB}	5,0	1,0	1,0	1,0	V
		V _{NLB}	10,0	2,0	2,0	2,0	V
		V _{NLB}	15,0	2,5	2,5	2,5	V

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25°C	T _{amb} HIGH	Unit
Noise margin at HIGH level output (equal to the difference between V _{IH} and V _{OH} for worst case combinations)		V _{NHB}	5,0	1,0	1,0	1,0	V
		V _{NHB}	10,0	2,0	2,0	2,0	V
		V _{NHB}	15,0	2,5	2,5	2,5	V
Propagation and Transition Times	C _L = 50pF (Test conditions as in Sub-group A5)						
Transition Time LOW to HIGH level		t _{TLHA}	5,0	-	360,0	-	ns
		t _{TLHA}	10,0	-	180,0	-	ns
		t _{TLHA}	15,0	-	130,0	-	ns
Transition Time HIGH to LOW level		t _{THLA}	5,0	-	200,0	-	ns
		t _{THLA}	10,0	-	100,0	-	ns
		t _{THLA}	15,0	-	80,0	-	ns
Clock Pulse Width (C1, Q1/C2 or PC inputs)		t _{PWCB}	5,0	-	250,0	-	ns
		t _{PWCB}	10,0	-	120,0	-	ns
		t _{PWCB}	15,0	-	90,0	-	ns
Clock Pulse Rise and Fall times (C1, Q1/C2 or PC inputs)		t _{rA} /	5,0	-	15,0	-	µs
		t _{fA}	10,0	-	15,0	-	µs
		t _{fA}	15,0	-	15,0	-	µs
Turn-Off Delay Time (PC and PCP outputs)		t _{PHLA}	5,0	-	1100,0	-	ns
		t _{PHLA}	10,0	-	390,0	-	ns
		t _{PHLA}	15,0	-	240,0	-	ns
Turn-On Delay Time (PC and PCP outputs)		t _{PLHA}	5,0	-	1350,0	-	ns
		t _{PLHA}	10,0	-	600,0	-	ns
		t _{PLHA}	15,0	-	380,0	-	ns
Counter D1							
Maximum Clock Pulse Frequency 4, 64 and 100 division ratio		Freq.A	5,0	-	3,0	-	MHz
		Freq.A	10,0	-	8,0	-	MHz
		Freq.A	15,0	-	10,0	-	MHz

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25°C	T _{amb} HIGH	Unit
Maximum Clock Pulse Frequency (contd)							
16 division ratio		Freq.A	5,0	-	1,0	-	MHz
		Freq.A	10,0	-	3,0	-	MHz
		Freq.A	15,0	-	5,0	-	MHz
Propagation Delay Time (Q1/C2 outputs) 4, 64 and 10 division ratio		t _{PLHA} / t _{PHLA}	5,0	-	900,0	-	ns
			10,0	-	380,0	-	ns
			15,0	-	260,0	-	ns
16 division ratio		t _{PLHA} / t _{PHLA}	5,0	-	1440,0	-	ns
			10,0	-	600,0	-	ns
			15,0	-	400,0	-	ns
<u>Counter D2</u>							
Maximum Clock Frequency		Freq.A	5,0	-	1,2	-	MHz
		Freq.A	10,0	-	3,0	-	MHz
		Freq.A	15,0	-	4,0	-	MHz
Turn-On Delay Time ('0' output)		t _{PLHA}	5,0	-	900,0	-	ns
		t _{PLHA}	10,0	-	380,0	-	ns
		t _{PLHA}	15,0	-	260,0	-	ns
Turn-Off Delay Time ('0' output)		t _{PHLA}	5,0	-	450,0	-	ns
		t _{PHLA}	10,0	-	170,0	-	ns
		t _{PHLA}	15,0	-	150,0	-	ns
Preset Enable Pulse Width		t _{PWPEA}	5,0	-	250,0	-	ns
		t _{PWPEA}	10,0	-	100,0	-	ns
		t _{PWPEA}	15,0	-	75,0	-	ns

Terminal identification

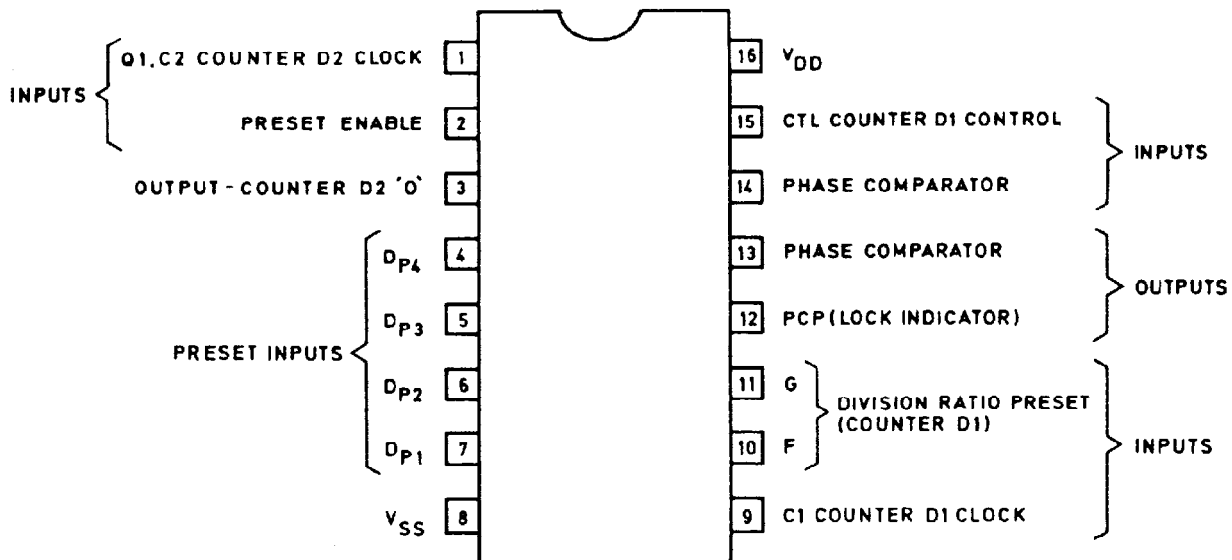


Figure 1

Function table

Table 1A

Counter D1

F PIN 10	G PIN 11	DIVISION RATIO OF COUNTER D1
L	L	4
L	H	16
H	L	64
H	H	100

Table 1B

Q1/C2	PE	DP1-DP4	'0' OUTPUT
	H	PRESET	COUNT DOWN '0' = H WHEN COUNT = ZERO
	L	X	COUNT
	X	X	NO ACTION

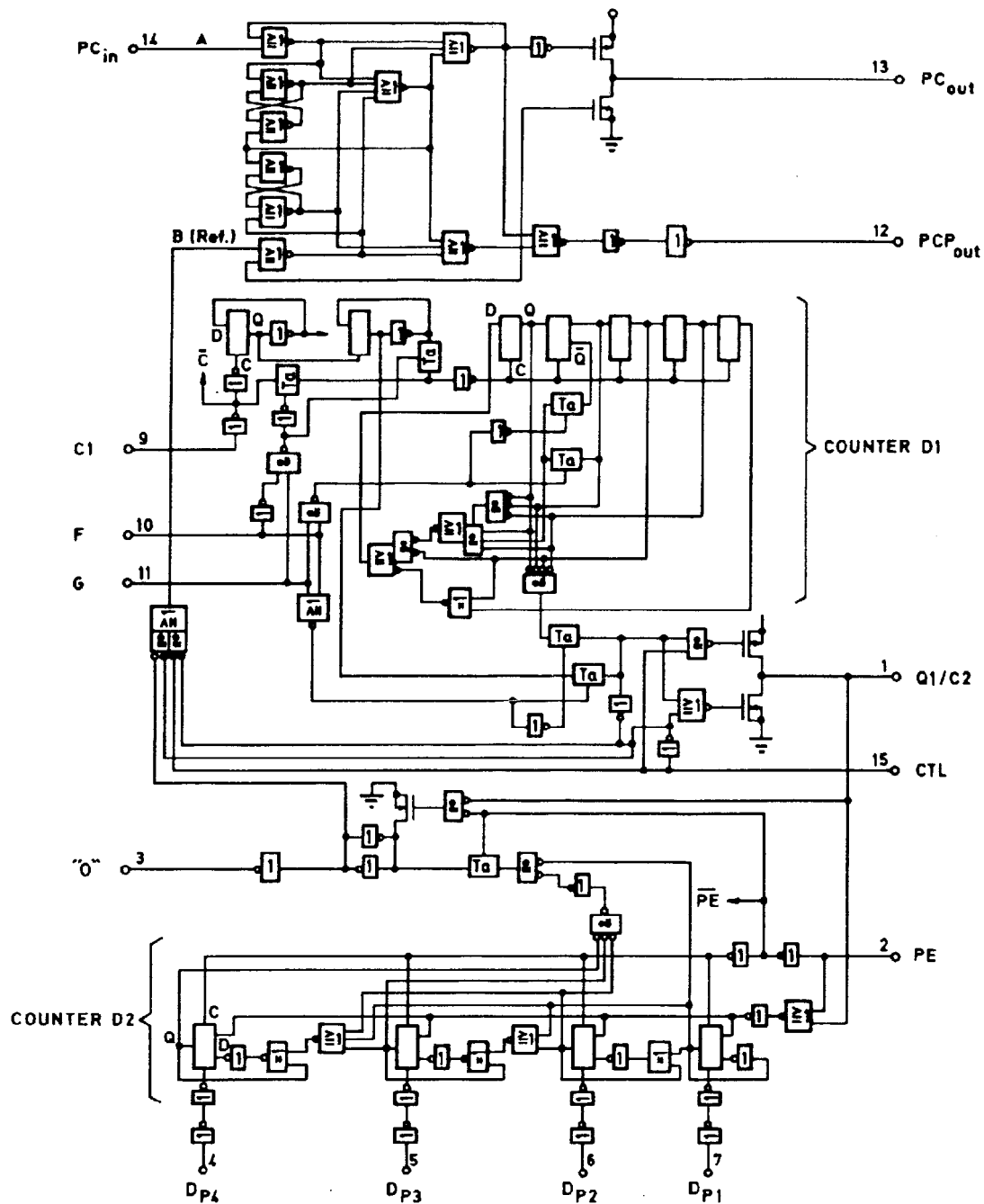
The divide-by-zero level on the programmable divide-by-N 4-bit binary counter, is illegal.

H = HIGH level

L = LOW level

X = Level irrelevant

Typical logic diagram



This is a graphic representation, not a circuit diagram

Figure 2

Switching time waveforms

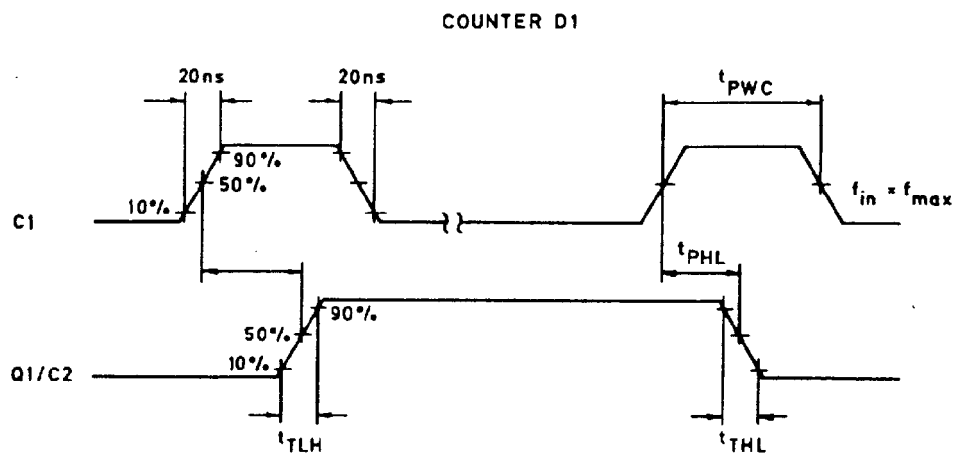
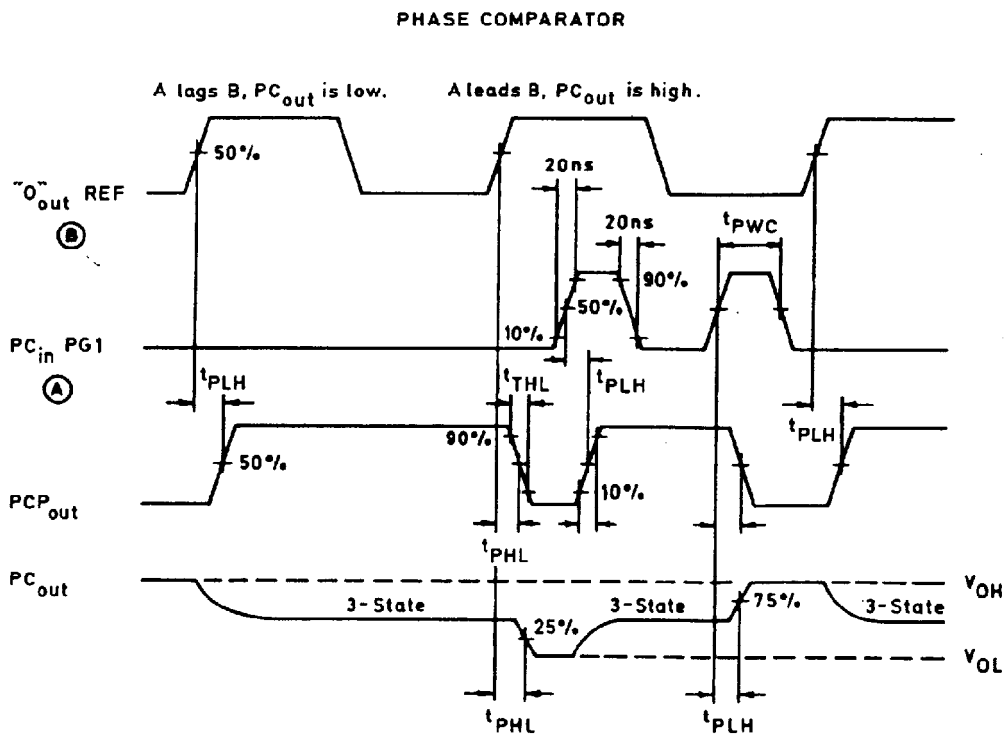


Figure 3