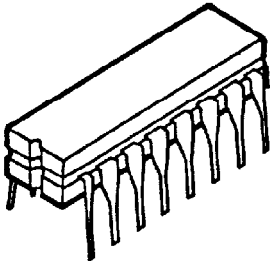


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON, W1A 2BS	BS CECC 90 104-206 ISSUE 1 JULY 1984. 
Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND MOTOROLA LTD, KELVIN ESTATE, EAST KILBRIDE. G75 0TG	Page 1 of 25 pages MANUFACTURERS TYPE NUMBER 4569B SEE PD 9002 AND CECC 00 200 For ordering information see page
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1982 BS CECC 90 100 : 1983 Outline not to scale: Isometric projection Marking information see page 8  For detail dimensions see IEC 191-2 (A50C)	HIGH SPEED PROGRAMMABLE DIVIDE-BY-N- DUAL 4-BIT BCD/BINARY COUNTER SILICON COMPLEMENTARY MOS. WITH (B) BUFFERED OUTPUTS AND CAVITY PACKAGING. Assessment levels R, T and V and optional screening categories A, B, C and D

CAUTION: THESE ARE STATIC SENSITIVE DEVICES - See clause 1.11

1. Limiting conditions of use (not for inspection purposes)

All voltages referenced to V_{SS}

1.1	Maximum supply voltage, positive	V_{DD}	+18,0V
1.2	Maximum supply voltage, negative	V_{DD}	-0,5V
1.3	Maximum positive input voltage	V_I	$V_{DD} + 0,5V$
1.4	Maximum negative input voltage	V_I	-0,5V

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1. Limiting conditions of use (cont'd)

1.5	Maximum power dissipation, per package per output	P_{D1}	200,0mW
		P_{D2}	100,0mW
1.6	Maximum continuous current into any input.	$ I_I $	10,0mA
1.7	Maximum continuous current into any output.	$ I_O $	10,0mA
1.8	Operating temperature range	T_{amb}	
		Full	-55 to +125 °C
		Limited	-40 to + 85 °C
1.9	Storage temperature range	T_{stg}	-65 to +150 °C
1.10	Transient energy rating		400V at 100pF through 1,5k Ω
1.11	<u>Recommended handling precautions</u>		
1.11.1	Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method.		
1.11.2	Use grounded tip soldering irons.		
1.11.3	Ground all test equipment.		
1.11.4	Connect all unused device inputs to V_{DD} or V_{SS} .		
1.11.5	PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations.		
1.11.6	Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices.		
1.11.7	Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during inspection or handling.		
1.11.8	When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage, 'Dummy connectors' should be used to electrically short all PC board terminals together.		
1.11.9	Switch off power supply before inserting or removing devices from circuits.		
1.11.10	Disconnect all low impedance equipment and input signals from the device before d.c. power supplies are switched off.		

2. Recommended conditions of use and associated characteristics (not for inspection purposes)

These apply over the operating temperature range unless otherwise stated. All voltages referenced to V_{SS} .

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25 °C	T_{amb} HIGH	Unit
Quiescent device current	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range	Outputs open circuit	I_{DDA}	5,0	5,0	5,0	150,0	μA
		I_{DDA}	10,0	10,0	10,0	300,0	μA
		I_{DDA}	15,0	20,0	20,0	600,0	μA
Limited temperature range		I_{DDA}	5,0	50,0	50,0	150,0	μA
		I_{DDA}	10,0	100,0	100,0	300,0	μA
		I_{DDA}	15,0	200,0	200,0	600,0	μA
LOW level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OLA}	5,0	0,05	0,05	0,05	V
		V_{OLA}	10,0	0,05	0,05	0,05	V
		V_{OLA}	15,0	0,05	0,05	0,05	V
HIGH level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OHB}	5,0	4,95	4,95	4,95	V
		V_{OHB}	10,0	9,95	9,95	9,95	V
		V_{OHB}	15,0	14,95	14,95	14,95	V
LOW level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IL} = 1,5V$	V_{OLA}	5,0	0,5	0,5	0,5	V
	$V_{IL} = 3,0V$	V_{OLA}	10,0	1,0	1,0	1,0	V
	$V_{IL} = 4,0V$	V_{OLA}	15,0	1,5	1,5	1,5	V
HIGH level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IH} = 3,5V$	V_{OHB}	5,0	4,5	4,5	4,5	V
	$V_{IH} = 7,0V$	V_{OHB}	10,0	9,0	9,0	9,0	V
	$V_{IH} = 11,0V$	V_{OHB}	15,0	13,5	13,5	13,5	V

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25 °C	T_{amb} HIGH	Unit
Output LOW (sink) current							
Full temperature range	$V_O = 0,4V$	I_{OLB}	5,0	0,64	0,51	0,36	mA
	$V_O = 0,5V$	I_{OLB}	10,0	1,60	1,30	0,90	mA
	$V_O = 1,5V$	I_{OLB}	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_O = 0,4V$	I_{OLB}	5,0	0,52	0,44	0,36	mA
	$V_O = 0,5V$	I_{OLB}	10,0	1,30	1,10	0,90	mA
	$V_O = 1,5V$	I_{OLB}	15,0	3,60	3,00	2,40	mA
Output HIGH (source) current							
Full temperature range	$V_O = 4,6V$	$-I_{OHB}$	5,0	0,25	0,51	0,14	mA
	$V_O = 9,5V$	$-I_{OHB}$	10,0	0,62	1,3	0,35	mA
	$V_O = 13,5V$	$-I_{OHB}$	15,0	1,80	3,4	1,10	mA
Limited temperature range	$V_O = 4,6V$	$-I_{OHB}$	5,0	0,2	0,44	0,12	mA
	$V_O = 9,5V$	$-I_{OHB}$	10,0	0,5	1,1	0,30	mA
	$V_O = 13,5V$	$-I_{OHB}$	15,0	1,4	3,0	1,00	mA
Input leakage current	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range		$ I_{IA} $	15,0	0,10	0,10	1,00	μA
Limited temperature range		$ I_{IA} $	15,0	0,30	0,30	1,00	μA
Input capacitance per unit load (Any input)	$V_I = 0V$ $f = 1MHz$	C_{IA}	-	-	7,5	-	pF
Noise margin at LOW level output (equal to the difference between V_{IL} and V_{OL} for worst case combinations)		V_{NLB}	5,0	1,0	1,0	1,0	V
		V_{NLB}	10,0	2,0	2,0	2,0	V
		V_{NLB}	15,0	2,5	2,5	2,5	V

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25 °C	T _{amb} HIGH	Unit
Noise margin at HIGH level output (equal to the difference between V _{IH} and V _{OH} for worst case combinations)		V _{NHB} V _{NHB} V _{NHB}	5,0 10,0 15,0	1,0 2,0 2,5	1,0 2,0 2,5	1,0 2,0 2,5	V V V
Propagation and transition times	C _L = 50pF (Test conditions as in Sub-group A5)						
Transition Time LOW to HIGH level		t _{TLHA} t _{TLHA} t _{TLHA}	5,0 10,0 15,0	- - -	200,0 100,0 80,0	- - -	ns ns ns
Transition Time HIGH to LOW level		t _{THLA} t _{THLA} t _{THLA}	5,0 10,0 15,0	- - -	200,0 100,0 80,0	- - -	ns ns ns
Propagation Delay Time LOW to HIGH level PE _{OUT}		t _{PLHA} t _{PLHA} t _{PLHA}	5,0 10,0 15,0	- - -	700,0 300,0 250,0	- - -	ns ns ns
Propagation Delay Time HIGH to LOW level PE _{OUT}		t _{PHLA} t _{PHLA} t _{PHLA}	5,0 10,0 15,0	- - -	600,0 300,0 200,0	- - -	ns ns ns
Propagation Delay Time LOW to HIGH level Q Output		t _{PLHA} t _{PLHA} t _{PLHA}	5,0 10,0 15,0	- - -	1200,0 500,0 400,0	- - -	ns ns ns
Propagation Delay Time HIGH to LOW level Q Output		t _{PHLA} t _{PHLA} t _{PHLA}	5,0 10,0 15,0	- - -	1000,0 400,0 300,0	- - -	ns ns ns

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25 °C	T _{amb} HIGH	Unit
Clock Pulse Width		t _{PWCB}	5,0	-	300,0	-	ns
		t _{PWCB}	10,0	-	150,0	-	ns
		t _{PWCB}	15,0	-	115,0	-	ns
Clock Rise and Fall Time		t _{rA} , t _{fA}	5,0	-	No Limit	-	µs
		t _{rA} , t _{fA}	10,0	-	No Limit	-	µs
		t _{rA} , t _{fA}	15,0	-	No Limit	-	µs
Clock Pulse Frequency		Freq.A	5,0	-	2,5	-	MHz
		Freq.A	10,0	-	5,7	-	MHz
		Freq.A	15,0	-	7,8	-	MHz

Terminal identification

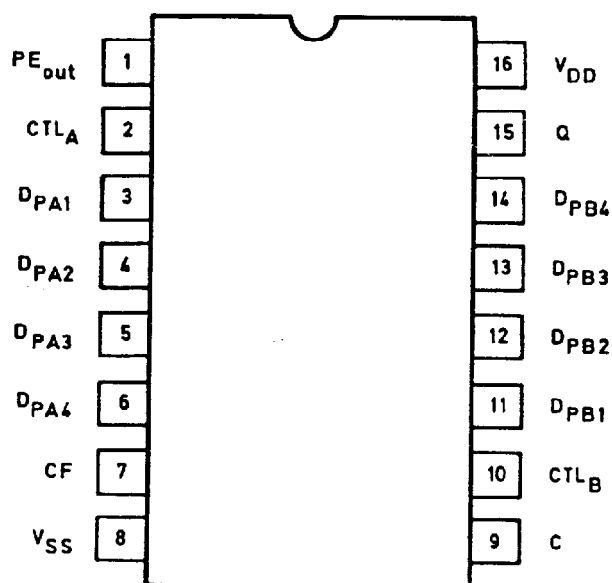


Figure 1

TYPICAL LOGIC DIAGRAM

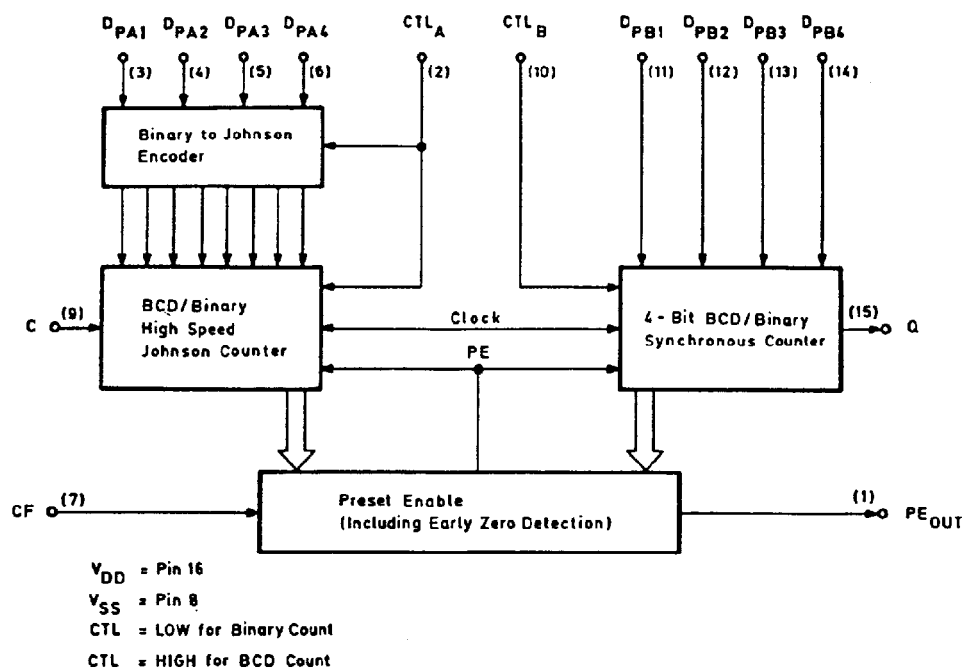


Figure 2

This is a graphic representation not a circuit diagram

SWITCHING TIME WAVEFORMS

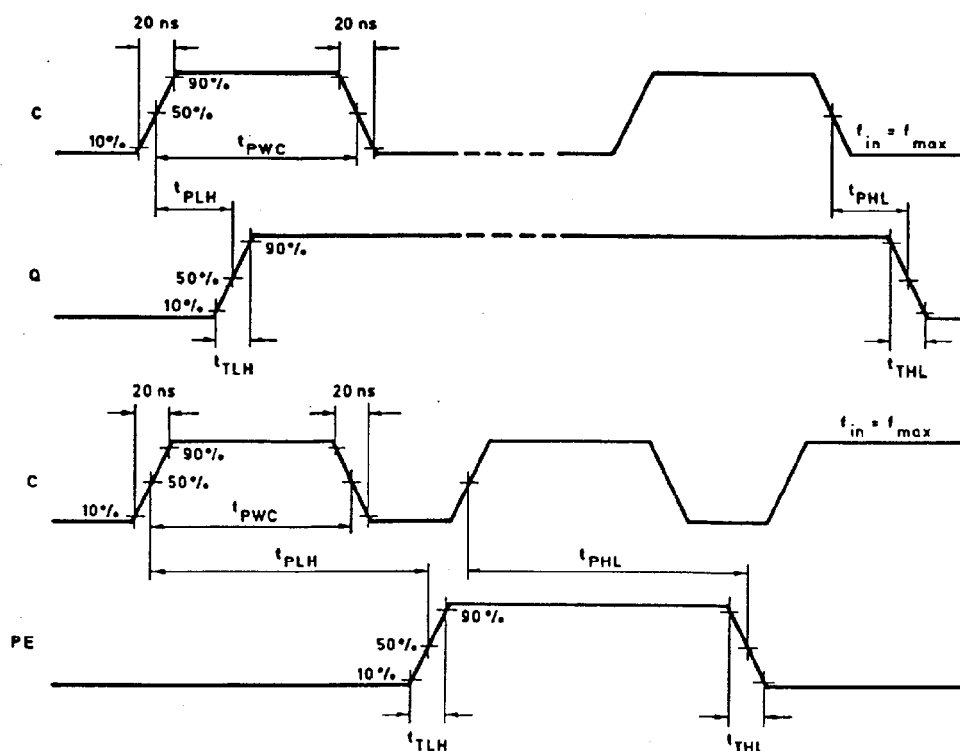


Figure 3

FUNCTIONAL DESCRIPTION

The 4569B includes a high speed Johnson counter followed by a BCD/binary 4-bit synchronous counter (see Function Block Diagram). The use of an encoder allows the Johnson counter to be programmed (i.e. preset) in BCD or binary code through inputs D_{PA1} , D_{PA2} , D_{PA3} , and D_{PA4} .

The BCD/binary counter can be programmed through inputs D_{PB1} , D_{PB2} , D_{PB3} , and D_{PB4} . For each counter a divide ratio of 10 (BCD count) or 16 (binary count) can be chosen independently by inputs CTL_A and CTL_B respectively. When one of those inputs is set HIGH, the divide ratio of the corresponding counter is 10 (BCD); when it is set LOW, the division ratio is 16 (binary).

A Cascade Feedback input (Pin 7), a Q output (Pin 15) and a Preset Enable output (Pin 1) made it possible to cascade the 4568B, 4522B and 4526B with this device, CF, Q and PE_{OUT} of 4569B must be respectively connected to LOW, C and PE of the following counter.

When 4569B is used alone, CF must be connected to V_{DD} . One pulse will appear on output PE_{OUT} every N clock periods (N being the value programmed on the D_p inputs).

Both counters included in 4569B, and eventually all the counters which are cascaded, should normally be preset at the programmed values during the clock period where they all reach the count zero. For best speed performance, preset is started as soon as count 1 is detected. As a consequence, it is not possible to program a frequency division ratio of one. However, it is possible to program a division ratio of 11 (i.e. $D_{PA1}, \dots, D_{PA4} = 1, 0, 0, 0$ and $D_{PB1}, \dots, D_{PB4} = 1, 0, 0, 0$), or a division ratio of 101 if another counter is cascaded with the 4569B.

This high speed configuration makes it possible to guarantee a maximum clock pulse frequency of 5.7 MHz for a 10V V_{DD} supply for any division ratio greater than one.

Due to the presence of the early zero detection, the circuit must be used in the two least significant digit positions.

Because all the circuitry is static, there is no minimum frequency specification for the Clock input, C (Pin 9).

MARKING

The following shall be marked on the device, in the following order of precedence, as space permits. All information, except the terminal marking shall appear on the primary package used as initial protection or wrapping for delivery:

- (1) Terminal identification
- (2) Type number
- (3) Operating temperature range (if not included in 2)
- (4) Quality assessment level applied
- (5) Screening class applied
- (6) Date-code (year-week defined by three or four figures)
- (7) Mark of conformity (CECC logo)
- (8) Manufacturers name or trade mark (may include factory code)
- (9) Factory identification code
- (10) Package materials
- (11) Caution label for devices susceptible to damage by electrostatic discharge