

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON. W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 AND

BS CECC 90 104 - 210

ISSUE 1

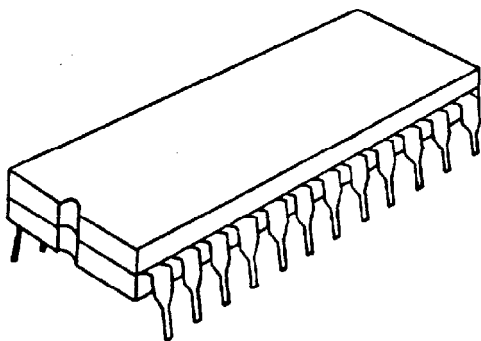
DECEMBER 1982



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ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:BS CECC 90 000 : 1976
BS CECC 90 100 : 1977

MANUFACTURERS TYPE NUMBER

4534BSEE PD 9002 AND CECC 00 200
For ordering information
see page 14Outline not to scale: Isometric projection
Marking information see page 13

For detail dimensions see IEC 191-2 (A51D)

REAL TIME 5 DECADE
COUNTER WITH 3-STATE
OUTPUTSSILICON COMPLEMENTARY MOS.
WITH (B) BUFFERED OUTPUTS AND
CAVITY PACKAGING.Assessment levels
R, S, T and V
and optional screening
categories A, B, C and D**CAUTION: THESE ARE STATIC SENSITIVE DEVICES - See clause 1.11****1 Limiting conditions of use (not for inspection purposes)**All voltages referenced to V_{SS}

1.1	Maximum supply voltage, positive	V_{DD}	+18,0V
1.2	Maximum supply voltage, negative	V_{DD}	-0,5V
1.3	Maximum positive input voltage	V_I V_{DD}	+0,5V
1.4	Maximum negative input voltage	V_I	-0,5V

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1. Limiting conditions of use (contd)

1.5	Maximum power dissipation, per package per output	P_{D1}	200,0mW
		P_{D2}	33,0mW
1.6	Maximum continuous current into any input.	$ I_I $	10,0mA
1.7	Maximum continuous current into any output.	$ I_O $	10,0mA
1.8	Operating temperature range	T_{amb}	
		Full	-55 to +125°C
		Limited	-40 to + 85°C
1.9	Storage temperature range	T_{stg}	-65 to +150°C
1.10	Transient energy rating		400V at 100pF through 1,5kΩ

1.11 Recommended handling precautions

- 1.11.1 Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method.
- 1.11.2 Use grounded tip soldering irons.
- 1.11.3 Ground all test equipment.
- 1.11.4 Connect all unused device inputs to V_{DD} or V_{SS} .
- 1.11.5 PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations.
- 1.11.6 Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices.
- 1.11.7 Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during inspection or handling.
- 1.11.8 When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage, 'Dummy connectors' should be used to electrically short all PC board terminals together.
- 1.11.9 Switch off power supply before inserting or removing devices from circuits.
- 1.11.10 Disconnect all low impedance equipment and input signals from the device before d.c. power supplies are switched off.

2. Recommended conditions of use and associated characteristics (not for inspection purposes)

These apply over the operating temperature range unless otherwise stated. All voltages referenced to V_{SS} .

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Quiescent device current	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range	Outputs open circuit	I_{DDA}	5,0	5,0	5,0	150,0	μA
		I_{DDA}	10,0	10,0	10,0	300,0	μA
		I_{DDA}	15,0	20,0	20,0	600,0	μA
Limited temperature range		I_{DDA}	5,0	50,0	50,0	375,0	μA
		I_{DDA}	10,0	100,0	100,0	750,0	μA
		I_{DDA}	15,0	200,0	200,0	1500,0	μA
LOW level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OLA}	5,0	0,05	0,05	0,05	V
		V_{OLA}	10,0	0,05	0,05	0,05	V
		V_{OLA}	15,0	0,05	0,05	0,05	V
HIGH level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OHB}	5,0	4,95	4,95	4,95	V
		V_{OHB}	10,0	9,95	9,95	9,95	V
		V_{OHB}	15,0	14,95	14,95	14,95	V
LOW level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IL} = 1,5V$ $V_{IL} = 3,0V$ $V_{IL} = 4,0V$	V_{OLA}	5,0	0,5	0,5	0,5	V
		V_{OLA}	10,0	1,0	1,0	1,0	V
		V_{OLA}	15,0	1,5	1,5	1,5	V
HIGH level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IH} = 3,5V$ $V_{IH} = 7,0V$ $V_{IH} = 11,0V$	V_{OHB}	5,0	4,5	4,5	4,5	V
		V_{OHB}	10,0	9,0	9,0	9,0	V
		V_{OHB}	15,0	13,5	13,5	13,5	V
Output LOW (sink) current							
Full temperature range	$V_O = 0,4V$	I_{OLB}	5,0	0,64	0,51	0,36	mA
	$V_O = 0,5V$	I_{OLB}	10,0	1,60	1,30	0,90	mA
	$V_O = 1,5V$	I_{OLB}	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_O = 0,4V$	I_{OLB}	5,0	0,52	0,44	0,36	mA
	$V_O = 0,5V$	I_{OLB}	10,0	1,30	1,10	0,90	mA
	$V_O = 1,5V$	I_{OLB}	15,0	3,60	3,00	2,40	mA

2. Recommended conditions of use and associated characteristics (contd)

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Output LOW (sink) current (Pins 1 and 22)							
Full temperature range	$V_O = 0,4V$	I_{OLB}	5,0	0,024	0,10	0,014	mA
	$V_O = 0,5V$	I_{OLB}	10,0	0,060	0,10	0,035	mA
	$V_O = 1,5V$	I_{OLB}	15,0	1,300	0,30	0,175	mA
Limited temperature range	$V_O = 0,4V$	I_{OLB}	5,0	0,012	0,010	0,008	mA
	$V_O = 0,5V$	I_{OLB}	10,0	0,030	0,025	0,020	mA
	$V_O = 1,5V$	I_{OLB}	15,0	0,140	0,120	0,100	mA
Output HIGH (source) current							
Full temperature range	$V_O = 4,6V$	$-I_{OHB}$	5,0	0,25	0,20	0,14	mA
	$V_O = 9,5V$	$-I_{OHB}$	10,0	0,62	0,50	0,35	mA
	$V_O = 13,5V$	$-I_{OHB}$	15,0	1,82	1,50	1,10	mA
Limited temperature range	$V_O = 4,6V$	$-I_{OHB}$	5,0	0,20	0,16	0,12	mA
	$V_O = 9,5V$	$-I_{OHB}$	10,0	0,50	0,40	0,30	mA
	$V_O = 13,5V$	$-I_{OHB}$	15,0	1,40	1,20	1,00	mA
Output HIGH (source) current (Pins 1 and 22)							
Full temperature range	$V_O = 4,6V$	$-I_{OHB}$	5,0	0,31	0,25	0,17	mA
	$V_O = 9,5V$	$-I_{OHB}$	10,0	0,31	0,25	0,17	mA
	$V_O = 13,5V$	$-I_{OHB}$	15,0	0,90	0,75	0,51	mA
Limited temperature range	$V_O = 4,6V$	$-I_{OHB}$	5,0	0,024	0,020	0,014	mA
	$V_O = 9,5V$	$-I_{OHB}$	10,0	0,060	0,050	0,035	mA
	$V_O = 13,5V$	$-I_{OHB}$	15,0	1,300	0,250	0,175	mA
Input leakage current	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range		$ I_{IA} $	15,0	$\pm 0,10$	$\pm 0,10$	$\pm 1,00$	μA
Limited temperature range		$ I_{IA} $	15,0	$\pm 0,30$	$\pm 0,30$	$\pm 1,00$	μA

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25°C	T _{amb} HIGH	Unit
Three state output leakage current (combined to obtain a high impedance output state)	V _{DisA} = V _{DD}						
Full temperature range		I _{OZA}	15,0	0,4	0,4	12,0	μA
Limited temperature range		I _{OZA}	15,0	1,6	1,6	12,0	μA
Input capacitance per unit load (Any input)	V _I = 0V f = 1MHz	C _{IA}	—	—	7,5	—	pF
Noise margin at LOW level output (equal to the difference between V _{IL} and V _{OL} for worst case combinations)		V _{NLB} V _{NLB} V _{NLB}	5,0 10,0 15,0	1,0 2,0 2,5	1,0 2,0 2,5	1,0 2,0 2,5	V V V
Noise margin at HIGH level output (equal to the difference between V _{IH} and V _{OH} for worst case combinations)		V _{NHB} V _{NHB} V _{NHB}	5,0 10,0 15,0	1,0 2,0 2,5	1,0 2,0 2,5	1,0 2,0 2,5	V V V
Propagation and Transition Times	C _L = 50pF (Test conditions as in Sub-group A5)						
Transition Time LOW to HIGH level		t _{TLHA} t _{TLHA} t _{TLHA}	5,0 10,0 15,0	— — —	360,0 180,0 130,0	— — —	ns ns ns
Transition Time HIGH to LOW level		t _{THLA} t _{THLA} t _{THLA}	5,0 10,0 15,0	— — —	200,0 100,0 80,0	— — —	ns ns ns
Propagation Delay Time Clock to Q		t _{PLHA} / t _{PHLA}	5,0 10,0 15,0	— — —	8,0 3,0 2,25	— — —	μs μs μs

2. Recommended conditions of use and associated characteristics (contd)

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25°C	T _{amb} HIGH	Unit
Clock to Carry out		t _{PLHA}	5,0	-	6,6	-	μs
		t _{PLHA}	10,0	-	2,5	-	μs
		t _{PLHA}	15,0	-	1,7	-	μs
Master Reset to Q		t _{PHLA}	5,0	-	3,6	-	μs
		t _{PHLA}	10,0	-	1,2	-	μs
		t _{PHLA}	15,0	-	0,9	-	μs
Master Reset to Error out		t _{PHLA}	5,0	-	1,50	-	μs
		t _{PHLA}	10,0	-	0,50	-	μs
		t _{PHLA}	15,0	-	0,38	-	μs
Scanner Clock to Q		t _{PLHA} /	5,0	-	3,6	-	μs
		t _{PHLA}	10,0	-	1,2	-	μs
			15,0	-	0,9	-	μs
Scanner Clock to Digit Select		t _{PLHA} /	5,0	-	3,0	-	μs
		t _{PHLA}	10,0	-	1,0	-	μs
			15,0	-	0,75	-	μs
Clock Pulse Frequency		f _{max.A}	5,0	-	0,5		MHz
		f _{max.A}	10,0	-	1,0		MHz
		f _{max.A}	15,0	-	1,2		MHz
Clock, or Scanner Clock Pulse Width		t _{PWCB}	5,0	-	1000,0	-	ns
		t _{PWCB}	10,0	-	500,0	-	ns
		t _{PWCB}	15,0	-	375,0	-	ns
Master Reset Pulse Width		t _{PWRB}	5,0	-	2000,0	-	ns
		t _{PWRB}	10,0	-	600,0	-	ns
		t _{PWRB}	15,0	-	450,0	-	ns
Three-state Propagation Delay Times Output HIGH to HIGH impedance		t _{PHZA*}	5,0	-	320,0	-	ns
		t _{PHZA*}	10,0	-	170,0	-	ns
			15,0	-	110,0	-	ns

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Three-state Propagation Delay Times (contd)							
Output LOW to High impedance		t_{PLZA}^*	5,0	-	320,0	-	ns
		t_{PLZA}^*	10,0	-	170,0	-	ns
		t_{PLZA}^*	15,0	-	110,0	-	ns
High impedance to HIGH level		t_{PZHA}^*	5,0	-	520,0	-	ns
		t_{PZHA}^*	10,0	-	210,0	-	ns
		t_{PZHA}^*	15,0	-	160,0	-	ns
High impedance to LOW level		t_{PZLA}^*	5,0	-	520,0	-	ns
		t_{PZLA}^*	10,0	-	210,0	-	ns
		t_{PZLA}^*	15,0	-	160,0	-	ns

*BCD and Digit Select Outputs only, using 3-state-control.

Terminal identification

(Viewed from above)

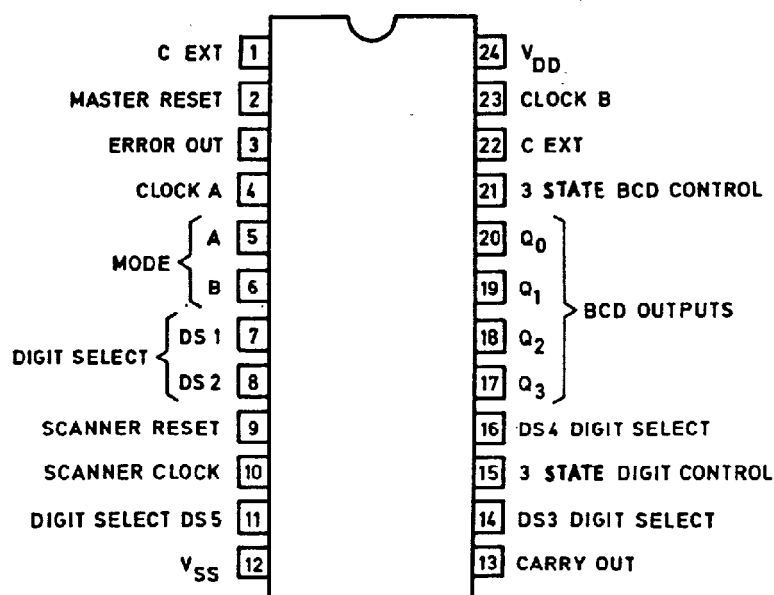


Figure 1

Function Tables
(Positive Logic)

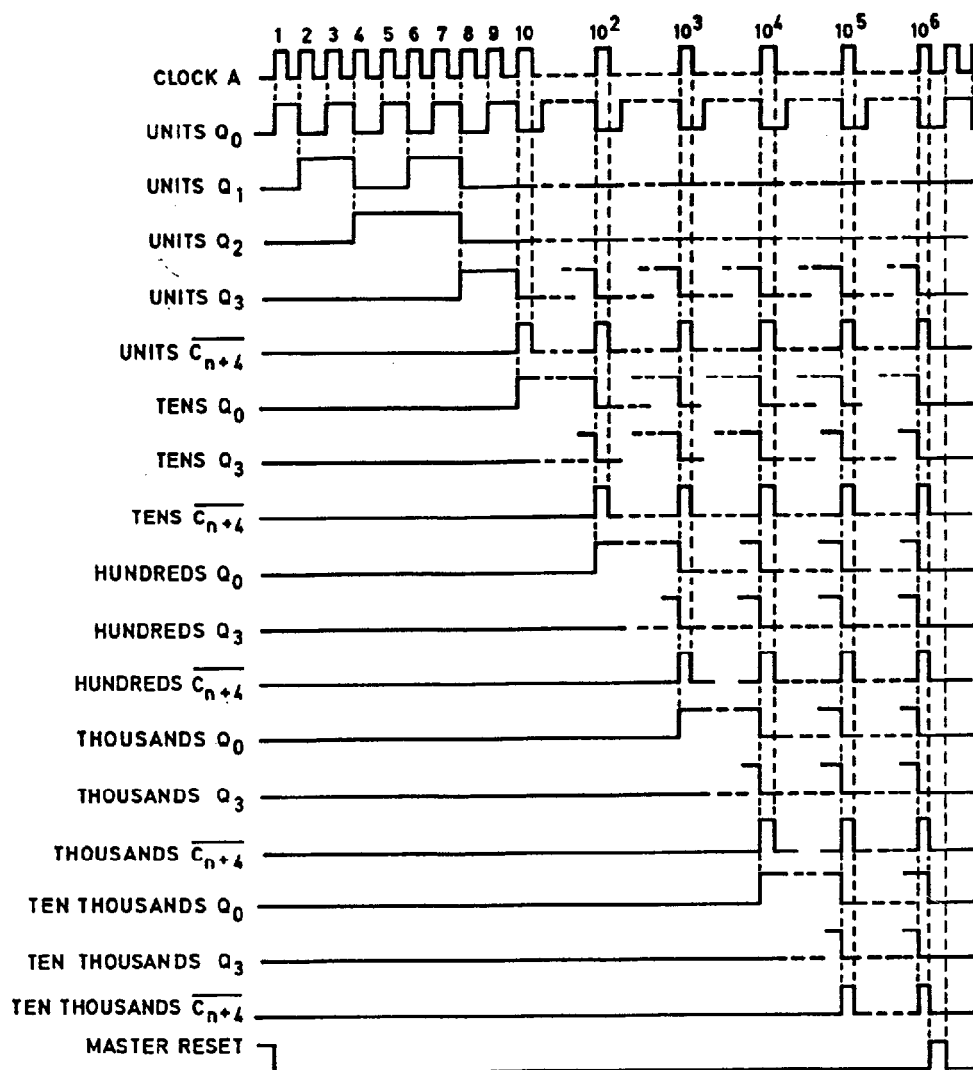
Table 1A

3-State Control	Out
LOW	Q or DS
HIGH	High impedance

Table 1B

Mode A	Mode B	First Decade Count	Carry to Second Stage	Application
LOW	LOW	Normal Count and Display	At 9 to 0 transition of first decade	5-Decade Counter
LOW	HIGH	Inhibited	Input Clock	Test Mode: Clock directly into stages 1, 2 and 4.
HIGH	HIGH	Inhibited	At 4 to 5 transition of first decade	4-decade counter with + 10 and roundoff at front end
HIGH	LOW	Counts 3,4,5,6,7 = 5 Counts 8,9,0,1,2 = 0	At 7 to 8 transition of first decade	4-decade counter with 1/2 pence capability

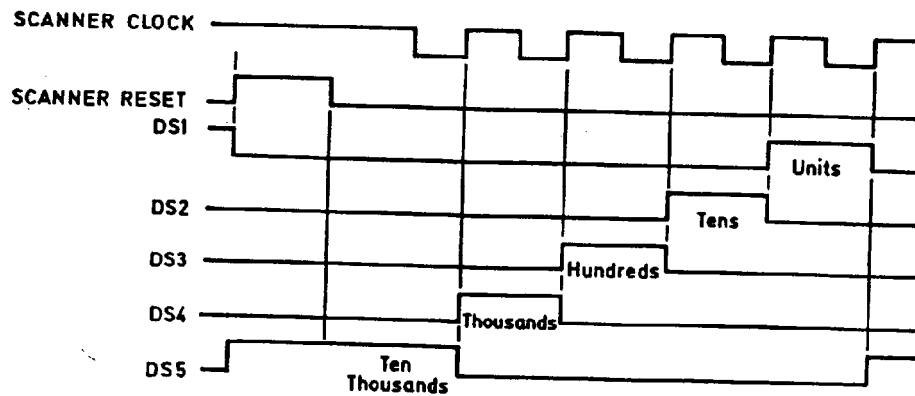
Timing diagrams



Counter Timing Diagram

Figure 2

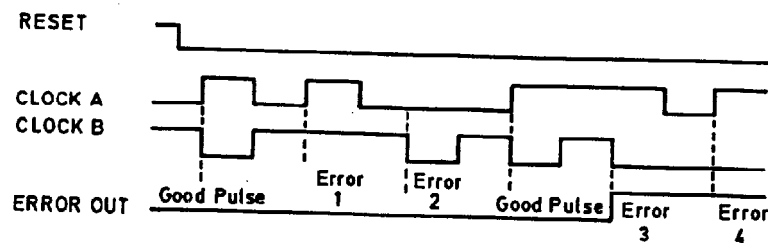
Timing diagrams (contd)



NOTE: If Mode B = HIGH, the first decade is inhibited and S1 will not go HIGH, and the cycle will be shortened to four stages. DS5 is selected automatically when Scanner Reset goes HIGH.

SCANNER TIMING DIAGRAM

Figure 3



NOTE: Error detector looks for inverted pulse on Clock B. Whenever a positive edge at Clock A is not accompanied by a negative pulse at Clock B (or vice-versa) within a time period of the one-shots an error is counted. Three errors result in Error Out to go to a HIGH. If error detection is not needed, tie Clock B HIGH or LOW and leave Pins 1 and 22 unconnected.

ERROR DETECTION TIMING DIAGRAM

Figure 4