

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON, W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 ANDMOTOROLA LTD,
KELVIN ESTATE,
EAST KILBRIDE.
G75 0TG

BS CECC 90 104- 213

ISSUE 1

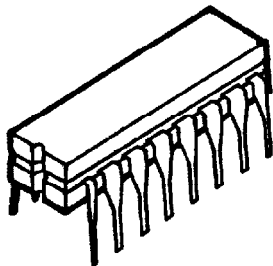
MARCH 1985



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ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:BS CECC 90 000 : 1982
BS CECC 90 100 : 1983

MANUFACTURERS TYPE NUMBER

4060BSEE PD 9002 AND CECC 00 200
For ordering information
see pageOutline not to scale: Isometric projection
Marking information see page 1314-BIT BINARY COUNTER AND
OSCILLATORSILICON COMPLEMENTARY MOS.
WITH (B) BUFFERED OUTPUTS AND
CAVITY PACKAGING.Assessment levels
R, T and V
and optional screening
categories A, B, C and D

For detail dimensions see IEC 191-2 (A50C)

CAUTION: THESE ARE STATIC SENSITIVE DEVICES - See clause 1.111. Limiting conditions of use (not for inspection purposes)All voltages referenced to V_{SS}

1.1	Maximum supply voltage, positive	V_{DD}	+18,0 V
1.2	Maximum supply voltage, negative	V_{DD}	-0,5 V
1.3	Maximum positive input voltage	V_{IN}	V_{DD} +0,5 V
1.4	Maximum negative input voltage	V_{IN}	-0,5 V

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

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1. Limiting conditions of use (cont'd)

- | | | | |
|---------|--|------------------------------|------------------------------------|
| 1.5 | Maximum power dissipation, per package
per output | P_{D1}
P_{D2} | 945 mW
189 mW |
| 1.6 | Maximum continuous current into any input. | $ I_I $ | 10,0 mA |
| 1.7 | Maximum continuous current into any output. | $ I_O $ | 10,0 mA |
| 1.8 | Operating temperature range. | T_{amb}
Full
Limited | - 55 to +125 °C
- 40 to + 85 °C |
| 1.9 | Storage temperature range. | T_{stg} | - 65 to +150 °C |
| 1.10 | Transient energy rating. | | 400 V at 100 pF
through 1,5 kΩ |
| 1.11 | <u>Recommended handling precautions</u> | | |
| 1.11.1 | Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method. | | |
| 1.11.2 | Use ground tip soldering irons. | | |
| 1.11.3 | Ground all test equipment. | | |
| 1.11.4 | Connect all unused device inputs to V_{DD} or V_{SS} . | | |
| 1.11.5 | PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations. | | |
| 1.11.6 | Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices. | | |
| 1.11.7 | Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during inspection or handling. | | |
| 1.11.8 | When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage, 'Dummy connectors' should be used to electrically short all PC board terminals together. | | |
| 1.11.9 | Switch off power supply before inserting or removing devices from circuits. | | |
| 1.11.10 | Disconnect all low impedance equipment and input signals from the device before d.c. power supplies are switched off. | | |

2. Recommended conditions of use and associated characteristics
(not for inspection purposes)

These apply over the operating temperature range unless otherwise stated. All voltages referenced to V_{SS} .

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25 °C	T_{amb} HIGH	Unit
Quiescent device current	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$						
Full temperature range	Outputs open circuit	I_{DDA}	5,0	5,0	5,0	150,0	μA
		I_{DDA}	10,0	10,0	10,0	300,0	μA
		I_{DDA}	15,0	20,0	20,0	600,0	μA
Limited temperature range		I_{DDA}	5,0	20,0	20,0	150,0	μA
		I_{DDA}	10,0	40,0	40,0	300,0	μA
		I_{DDA}	15,0	80,0	80,0	600,0	μA
LOW level output voltage at $ I_O < 1,0 \mu A$	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$	V_{OLA}	5,0	0,05	0,05	0,05	V
		V_{OLA}	10,0	0,05	0,05	0,05	V
		V_{OLA}	15,0	0,05	0,05	0,05	V
HIGH level output voltage at $ I_O < 1,0 \mu A$	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$	V_{OHB}	5,0	4,95	4,95	4,95	V
		V_{OHB}	10,0	9,95	9,95	9,95	V
		V_{OHB}	15,0	14,95	14,95	14,95	V
LOW level output voltage (for worst case combinations) at $ I_O < 1,0 \mu A$	$V_{IL} = 1,5 V$	V_{OLA}	5,0	0,5	0,5	0,5	V
	$V_{IL} = 3,0 V$	V_{OLA}	10,0	1,0	1,0	1,0	V
	$V_{IL} = 4,0 V$	V_{OLA}	15,0	1,5	1,5	1,5	V
HIGH level output voltage (for worst case combinations) at $ I_O < 1,0 \mu A$	$V_{IH} = 3,5 V$	V_{OHB}	5,0	4,5	4,5	4,5	V
	$V_{IH} = 7,0 V$	V_{OHB}	10,0	9,0	9,0	9,0	V
	$V_{IH} = 11,0 V$	V_{OHB}	15,0	13,5	13,5	13,5	V

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25 °C	T_{amb} HIGH	Unit
Output LOW (sink) current							
Full temperature range	$V_0 = 0,4 V$	I_{OLB}	5,0	0,64	0,51	0,36	mA
	$V_0 = 0,5 V$	I_{OLB}	10,0	1,60	1,30	0,90	mA
	$V_0 = 1,5 V$	I_{OLB}	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_0 = 0,4 V$	I_{OLB}	5,0	0,52	0,44	0,36	mA
	$V_0 = 0,5 V$	I_{OLB}	10,0	1,30	1,10	0,90	mA
	$V_0 = 1,5 V$	I_{OLB}	15,0	3,60	3,00	2,40	mA
Output HIGH (source) current							
Full temperature range	$V_0 = 4,6 V$	$-I_{OHB}$	5,0	0,64	0,51	0,36	mA
	$V_0 = 9,5 V$	$-I_{OHB}$	10,0	1,60	1,30	0,90	mA
	$V_0 = 13,5 V$	$-I_{OHB}$	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_0 = 4,6 V$	$-I_{OHB}$	5,0	0,52	0,44	0,36	mA
	$V_0 = 9,5 V$	$-I_{OHB}$	10,0	1,30	1,10	0,90	mA
	$V_0 = 13,5 V$	$-I_{OHB}$	15,0	3,60	3,00	2,40	mA
Input leakage current	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$						
Full temperature range		$ I_{IA} $	15,0	0,10	0,10	1,00	μA
Limited temperature range		$ I_{IA} $	15,0	0,30	0,30	1,00	μA
Input capacitance per unit load (Any input)	$V_I = 0 V$ $f = 1 MHz$	C_{IA}	-	-	7,5	-	pF
Noise margin at LOW level output (equal to the difference between V_{IL} and V_{OL} for worst case combinations)		V_{NLB} V_{NLB} V_{NLB}	5,0 10,0 15,0	1,0 2,0 2,5	1,0 2,0 2,5	1,0 2,0 2,5	V V V

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = +25° C	T _{amb} HIGH	Unit
Noise margin at HIGH level output (equal to the difference between V _{IH} and V _{OH} for worst case combinations)		V _{NHB}	5,0	1,0	1,0	1,0	V
		V _{NHB}	10,0	2,0	2,0	2,0	V
		V _{NHB}	15,0	2,5	2,5	2,5	V
Propagation and Transition Times	C _L = 50 pF (Test conditions as in Sub-group A5)						
Propagation Delay Time LOW to HIGH and HIGH to LOW level Clock _{in} to Q4		t _{PLHA} / t _{PHLA}	5,0	-	740,0	-	ns
		t _{PLHA} / t _{PHLA}	10,0	-	300,0	-	ns
		t _{PLHA} / t _{PHLA}	15,0	-	200,0	-	ns
Propagation Delay Time LOW to HIGH and HIGH to LOW level Clock _{in} to Q14		t _{PLHA} / t _{PHLA}	5,0	-	2,7	-	μs
		t _{PLHA} / t _{PHLA}	10,0	-	1,3	-	μs
		t _{PLHA} / t _{PHLA}	15,0	-	1,0	-	μs
Propagation Delay Time HIGH to LOW Reset to Qn		t _{PHLA}	5,0	-	360,0	-	ns
		t _{PHLA}	10,0	-	160,0	-	ns
		t _{PHLA}	15,0	-	100,0	-	ns
Transition Times LOW to HIGH and HIGH to LOW level Counter Outputs		t _{TLHA} / t _{THLA}	5,0	-	200,0	-	ns
		t _{TLHA} / t _{THLA}	10,0	-	100,0	-	ns
		t _{TLHA} / t _{THLA}	15,0	-	80,0	-	ns

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = +25 °C	T _{amb} HIGH	Unit
Clock Pulse Width		t _{PWCB}	5,0	-	100,0	-	ns
		t _{PWCB}	10,0	-	40,0	-	ns
		t _{PWCB}	15,0	-	30,0	-	ns
Clock Pulse Frequency		f _{max.A}	5,0	-	3,5	-	MHz
		f _{max.A}	10,0	-	8,0	-	MHz
		f _{max.A}	15,0	-	12,0	-	MHz
Clock Rise and Fall Time		t _{rA} / t _{fA}	5,0	NO LIMIT			
		t _{rA} / t _{fA}	10,0				
		t _{rA} / t _{fA}	15,0				
Reset Pulse Width		t _{PWRB}	5,0	-	120,0	-	ns
		t _{PWRB}	10,0	-	60,0	-	ns
		t _{PWRB}	15,0	-	40,0	-	ns

Terminal Identification

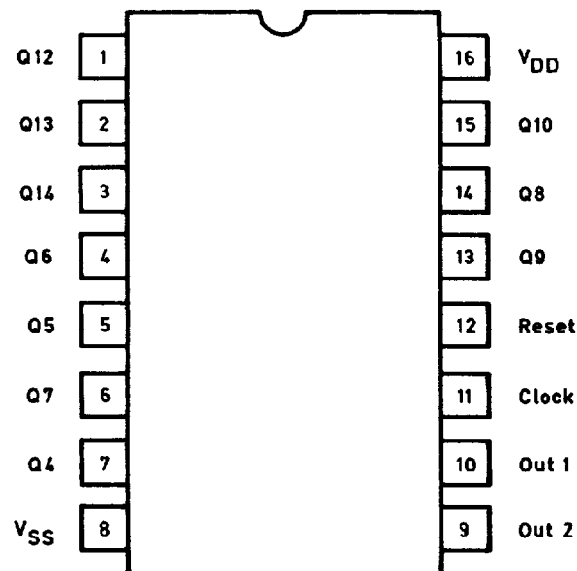


Figure 1

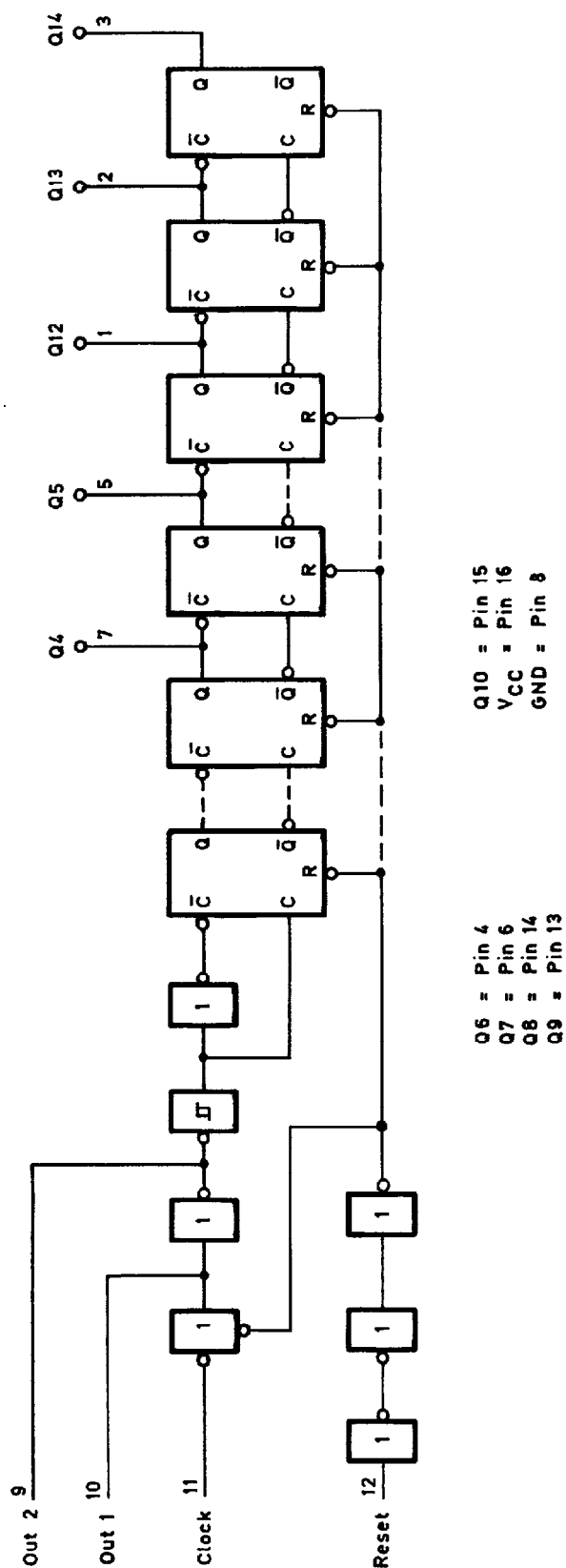
Function Table

Table 1

Clock _{in}	RESET	OUTPUT LEVEL
↗	L	No Change
↘	L	Advance to next level
X	H	All outputs are low

H = HIGH level
 L = LOW level
 X = Level irrelevant
 ↗ = Transition low to high level
 ↘ = Transition high to low level

Logic diagrams



This is a graphic representation not a circuit diagram.

Figure 2

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Power Dissipation Test Circuit and Waveform

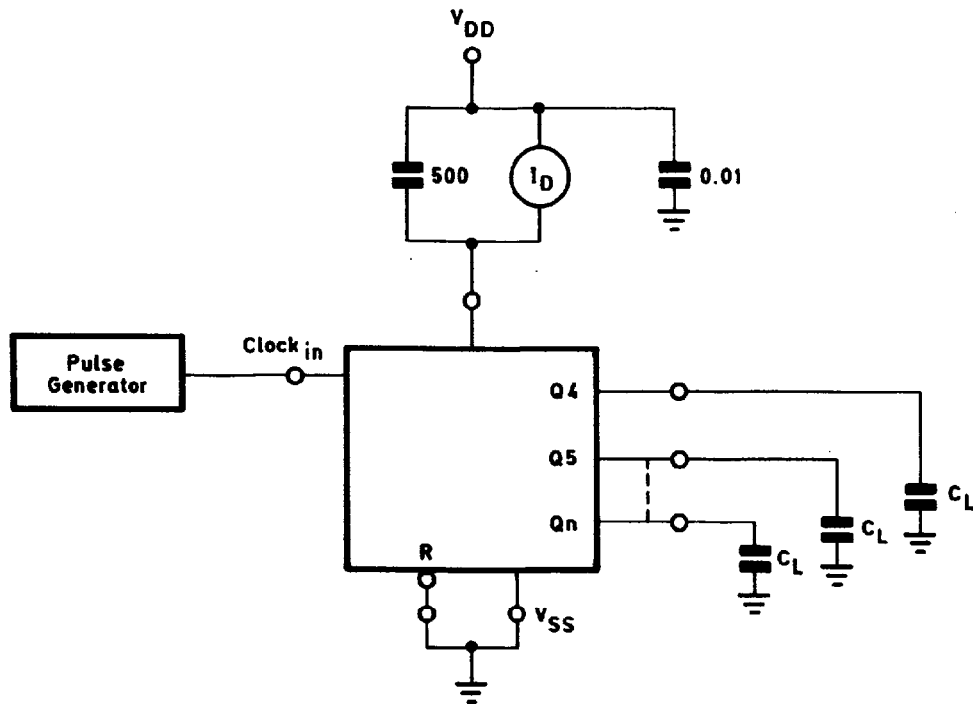


Figure 3a

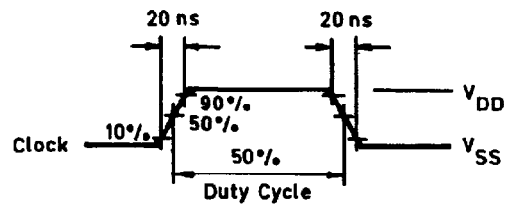


Figure 3b

Power Dissipation Test Circuit and Waveform (cont'd)

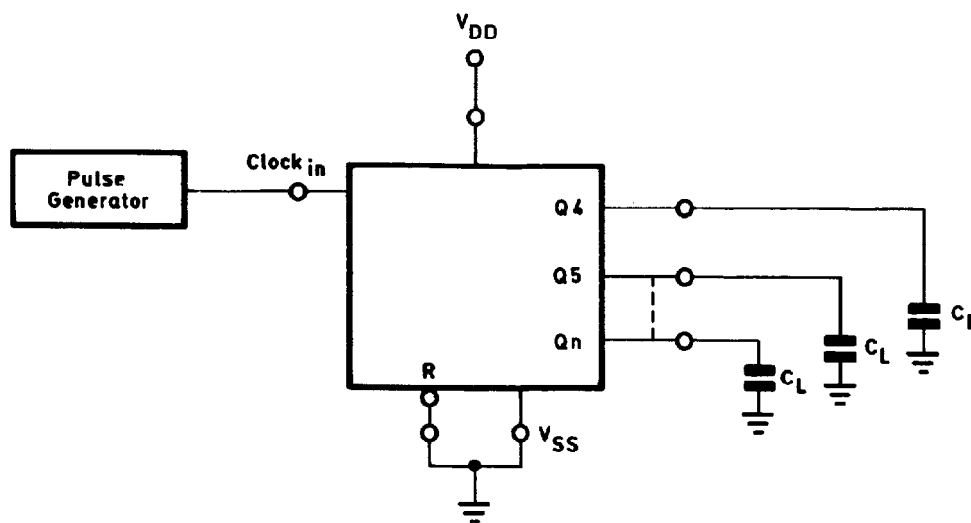


Figure 4a

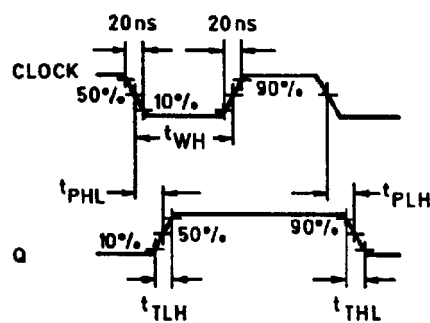
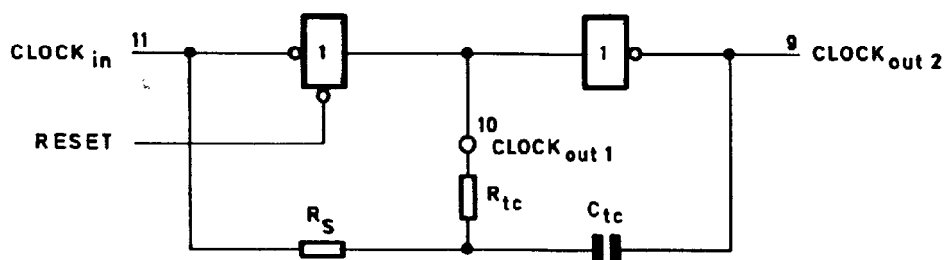


Figure 4b

Oscillator circuit using RC configuration



$$f = \frac{1}{2.3 R_{tc} C_{tc}} \quad \text{if } 1 \text{ kHz} \leq f \leq 100 \text{ kHz and } R_S \cong 2 R_{tc}$$

(f in Hz, R in ohms, C in farads)

Figure 5

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