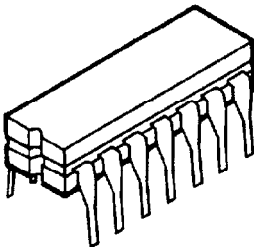


BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON, W1A 2BS Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND MOTOROLA LTD, KELVIN ESTATE, EAST KILBRIDE. G75 0TG	BS CECC 90 104-214 ISSUE 1 AUGUST 1985 Page 1 of 34 pages 
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1982 BS CECC 90 100 : 1983	MANUFACTURERS TYPE NUMBER 4093B SEE PD 9002 AND CECC 00 200 For ordering information see page 12
Outline not to scale: Isometric projection Marking information see page 11  For detail dimensions see IEC 191-2 (A50B)	QUAD 2-INPUT "NAND" SCHMITT TRIGGER SILICON COMPLEMENTARY MOS. WITH (B) BUFFERED OUTPUTS AND CAVITY PACKAGING. Assessment levels R, T and V and optional screening categories A, B, C and D

CAUTION: THESE ARE STATIC SENSITIVE DEVICES - See clause 1.11

1. Limiting conditions of use (not for inspection purposes)

All voltages referenced to V_{SS}

1.1	Maximum supply voltage, positive	V_{DD}	+18,0 V
1.2	Maximum supply voltage, negative	V_{DD}	-0,5 V
1.3	Maximum positive input voltage	V_{IN}	$V_{DD} + 0,5 V$
1.4	Maximum negative input voltage	V_{IN}	-0,5 V

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1. Limiting conditions of use (cont'd)

- | | | | |
|---------|---|-----------|-----------------------------------|
| 1.5 | Maximum power dissipation, per package | P_{D1} | 432 mW |
| | per output | P_{D2} | 108 mW |
| 1.6 | Maximum continuous current into any input. | $ I_I $ | 10,0 mA |
| 1.7 | Maximum continuous current into any output. | $ I_O $ | 10,0 mA |
| 1.8 | Operating temperature range | T_{amb} | |
| | | Full | -55 to +125 °C |
| | | Limited | -40 to + 85 °C |
| 1.9 | Storage temperature range | T_{stg} | -65 to +150 °C |
| 1.10 | Transient energy rating | | 400 V at 100 pF
through 1,5 kΩ |
| 1.11 | <u>Recommended handling precautions</u> | | |
| 1.11.1 | Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method. | | |
| 1.11.2 | Use grounded tip soldering irons. | | |
| 1.11.3 | Ground all test equipment. | | |
| 1.11.4 | Connect all unused device inputs to V_{DD} or V_{SS} | | |
| 1.11.5 | PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations. | | |
| 1.11.6 | Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices. | | |
| 1.11.7 | Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during inspection or handling. | | |
| 1.11.8 | When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage 'Dummy connectors' should be used to electrically short all PC board terminals together. | | |
| 1.11.9 | Switch off power supply before inserting or removing devices from circuits. | | |
| 1.11.10 | Disconnect all low impedance equipment and input signals from the device before d.c. power supplies are switched off. | | |

2. Recommended conditions of use and associated characteristics (not for inspection purposes)

These apply over the operating temperature range unless otherwise stated. All voltages referenced to V_{SS} .

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Quiescent device current	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$						
Full temperature range	Outputs open circuit	I_{DDA}	5,0	0,25	0,25	7,50	μA
		I_{DDA}	10,0	0,50	0,50	15,0	μA
		I_{DDA}	15,0	1,00	1,00	30,0	μA
Limited temperature range		I_{DDA}	5,0	1,00	1,00	7,50	μA
		I_{DDA}	10,0	2,00	2,00	15,0	μA
		I_{DDA}	15,0	4,00	4,00	30,0	μA
LOW level output voltage at $ I_O < 1,0 \mu A$	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$	V_{OLA}	5,0	0,05	0,05	0,05	V
		V_{OLA}	10,0	0,05	0,05	0,05	V
		V_{OLA}	15,0	0,05	0,05	0,05	V
HIGH level output voltage at $ I_O < 1,0 \mu A$	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$	V_{OHB}	5,0	4,95	4,95	4,95	V
		V_{OHB}	10,0	9,95	9,95	9,95	V
		V_{OHB}	15,0	14,95	14,95	14,95	V
LOW level output voltage (for worst case combinations) at $ I_O < 1,0 \mu A$	$V_{IL} = 1,5 V$ $V_{IL} = 3,0 V$ $V_{IL} = 4,0 V$	V_{OLA}	5,0	0,5	0,5	0,5	V
		V_{OLA}	10,0	1,0	1,0	1,0	V
		V_{OLA}	15,0	1,5	1,5	1,5	V
HIGH level output voltage (for worst case combinations) at $ I_O < 1,0 \mu A$	$V_{IH} = 3,5 V$ $V_{IH} = 7,0 V$ $V_{IH} = 11,0 V$	V_{OHB}	5,0	4,5	4,5	4,5	V
		V_{OHB}	10,0	9,0	9,0	9,0	V
		V_{OHB}	15,0	13,5	13,5	13,5	V
LOW level input voltage	$V_O = 4,5 V$ $V_O = 9,5 V$ $V_O = 13,5 V$	V_{ILA}	5,0	1,5	1,5	1,5	V
		V_{ILA}	10,0	3,0	3,0	3,0	V
		V_{ILA}	15,0	4,0	4,0	4,0	V
HIGH level input voltage	$V_O = 4,5 V$ $V_O = 9,5 V$ $V_O = 13,5 V$	V_{IHA}	5,0	3,5	3,5	3,5	V
		V_{IHA}	10,0	7,0	7,0	7,0	V
		V_{IHA}	15,0	11,0	11,0	11,0	V

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Output LOW (sink) current							
Full temperature range	$V_O = 0,4 V$	I_{OLB}	5,0	0,64	0,51	0,36	mA
	$V_O = 0,5 V$	I_{OLB}	10,0	1,60	1,30	0,90	mA
	$V_O = 1,5 V$	I_{OLB}	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_O = 0,4 V$	I_{OLB}	5,0	0,52	0,44	0,36	mA
	$V_O = 0,5 V$	I_{OLB}	10,0	1,30	1,10	0,90	mA
	$V_O = 1,5 V$	I_{OLB}	15,0	3,60	3,00	2,40	mA
Output HIGH (source) current							
Full temperature range	$V_O = 4,5 V$	$-I_{OHB}$	5,0	0,64	0,51	0,36	mA
	$V_O = 9,5 V$	$-I_{OHB}$	10,0	1,60	1,30	0,90	mA
	$V_O = 13,5 V$	$-I_{OHB}$	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_O = 4,5 V$	$-I_{OHB}$	5,0	0,53	0,44	0,36	mA
	$V_O = 9,5 V$	$-I_{OHB}$	10,0	1,30	1,10	0,90	mA
	$V_O = 13,5 V$	$-I_{OHB}$	15,0	3,60	3,00	2,40	mA
Input leakage current	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$						
Full temperature range		$ I_{IA} $	15,0	0,10	0,10	1,00	μA
Limited temperature range		$ I_{IA} $	15,0	0,30	0,30	1,00	μA
Input capacitance per unit load (Any input)	$V_I = 0 V$ $f = 1 MHz$	C_{IA}	-	-	7,5	-	pF
Noise margin at LOW level output (equal to the difference between V_{IL} and V_{OL} for worst case combinations)		V_{NLB}	5,0	1,0	1,0	1,0	V
		V_{NLB}	10,0	2,0	2,0	2,0	V
		V_{NLB}	15,0	2,5	2,5	2,5	V

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25°C	T _{amb} HIGH	UNIT
Noise margin at HIGH level output (equal to the difference between V _{IH} and V _{OH} for worst case combinations)		V _{NHB}	5,0	1,0	1,0	1,0	V
		V _{NHB}	10,0	2,0	2,0	2,0	V
		V _{NHB}	15,0	2,5	2,5	2,5	V
Hysteresis Voltage (Pins 1,5,8 and 12 held high or Pins 2,6, 9 and 13 held high)		V _H	5,0	0,20	0,17	0,13	V Min
		V _H	10,0	0,29	0,25	0,20	V Min
		V _H	15,0	0,39	0,33	0,27	V Min
		V _H	5,0	0,62	0,6	0,6	V Max
		V _H	10,0	0,85	0,8	0,8	V Max
		V _H	15,0	1,20	0,9	1,1	V Max
Threshold Voltage (Pins 2,5, 9 and 12, held high) Positive-Going Negative-Going		V _{T+}	5,0	1,90	1,80	1,70	V Min
		V _{T+}	10,0	3,05	2,95	2,85	V Min
		V _{T+}	15,0	4,12	4,02	3,95	V Min
		V _{T+}	5,0	4,15	4,05	4,05	V Max
		V _{T+}	10,0	6,75	6,65	6,65	V Max
		V _{T+}	15,0	9,15	9,05	9,05	V Max
		V _{T-}	5,0	1,63	1,63	1,53	V Min
		V _{T-}	10,0	2,70	2,70	2,60	V Min
		V _{T-}	15,0	3,59	3,69	3,70	V Min
		V _{T-}	5,0	3,76	3,66	3,66	V Max
		V _{T-}	10,0	6,18	6,08	6,08	V Max
		V _{T-}	15,0	8,40	8,30	8,30	V Max

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25°C	T _{amb} HIGH	UNIT
Propagation Delay Time LOW to HIGH and HIGH to LOW level		t _{PLHA} / t _{PHLA}	5,0	-	250,0	-	ns
		t _{PLHA} / t _{PHLA}	10,0	-	100,0	-	ns
		t _{PLHA} / t _{PHLA}	15,0	-	80,0	-	ns
Transition Time LOW to HIGH and HIGH to LOW level		t _{TLHA} / t _{THLA}	5,0	-	200,0	-	ns
		t _{TLHA} / t _{THLA}	10,0	-	100,0	-	ns
		t _{TLHA} / t _{THLA}	15,0	-	80,0	-	ns

TABLE 1

INPUT		OUTPUT
A	B	Y
H	H	L
L	X	H

H = High level
L = Low level
X = Level Irrelevant

Terminal identification

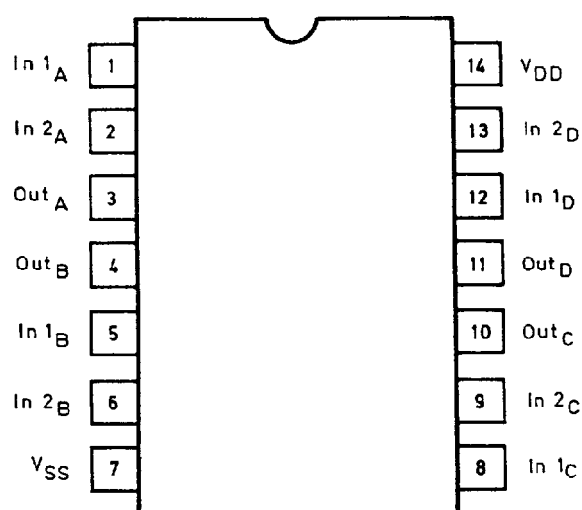


Figure 1

Logic diagram

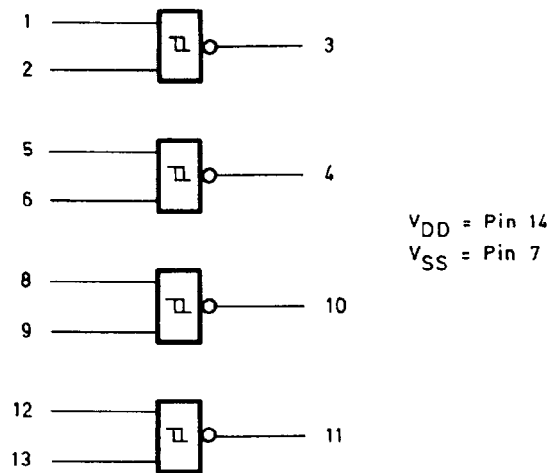


Figure 2

Switching Waveforms

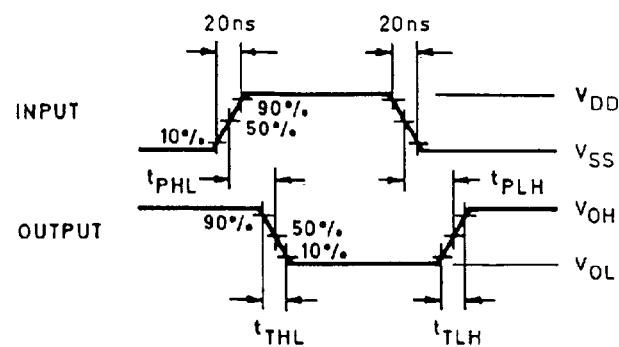


Figure 3

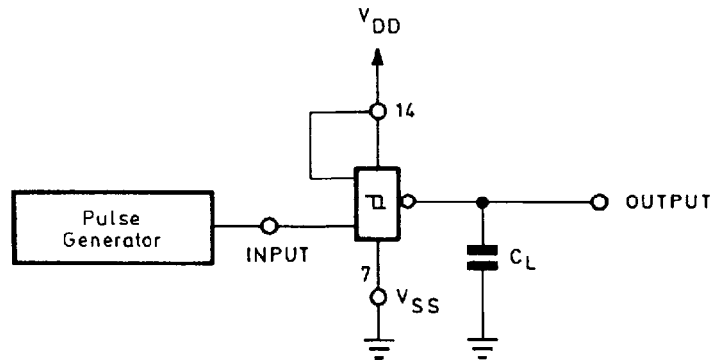


Figure 4

Typical Schmitt Trigger applications.

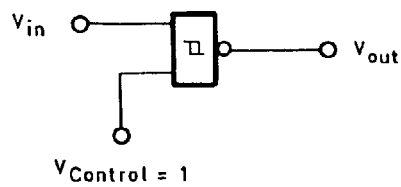


Figure 5

Schmitt Trigger will square up inputs with
slow rise and fall times.

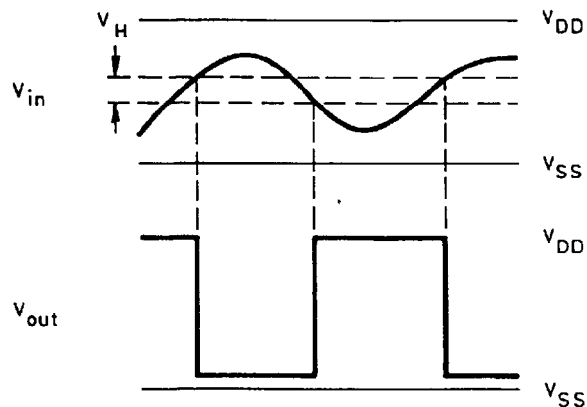


Figure 6

A Schmitt trigger offers maximum
noise immunity in gate applications.

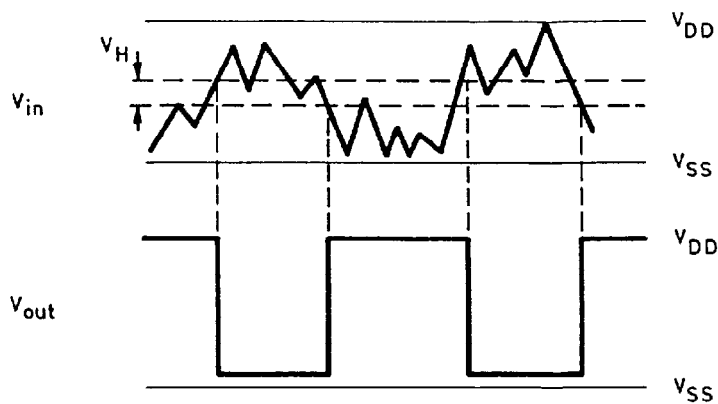


Figure 7

Typical Output Source Characteristics Test Circuit.

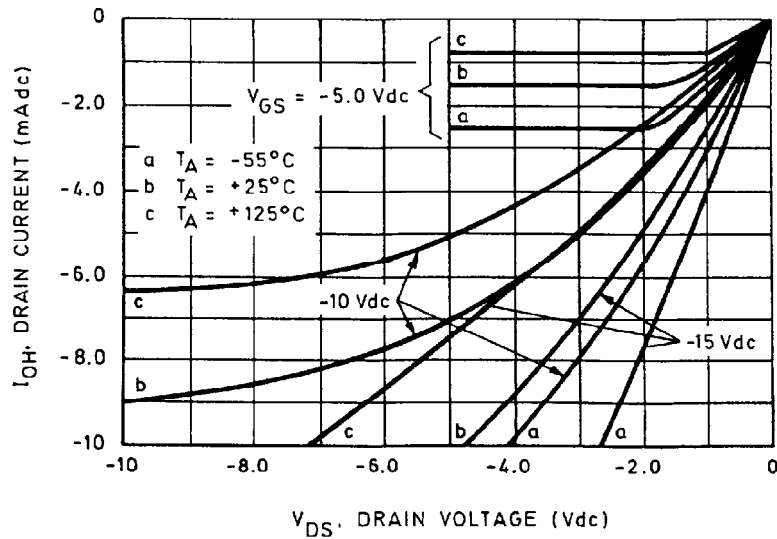
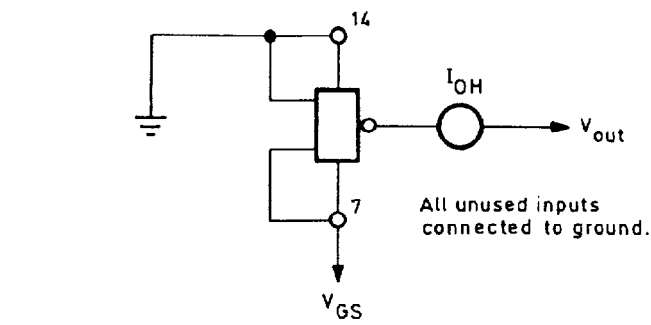


Figure 8