

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON, W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 ANDMOTOROLA LTD,
KELVIN ESTATE,
EAST KILBRIDE.
G75 OTG

BS CECC 90 104 - 215

ISSUE 1

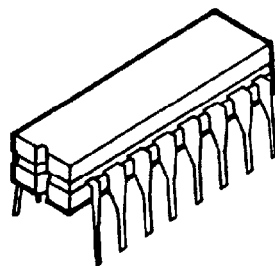
AUGUST 1983



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ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:BS CECC 90 000 : 1982
BS CECC 90 100 : 1983

MANUFACTURERS TYPE NUMBER

4504BSEE PD 9002 AND CECC 00 200
For ordering information
see page 10Outline not to scale: Isometric projection
Marking information see page 10TTL or CMOS to CMOS HEX LEVEL
SHIFTERSILICON COMPLEMENTARY MOS.
WITH (B) BUFFERED OUTPUTS AND
CAVITY PACKAGING.Assessment levels
R, T and V
and optional screening
categories A, B, C and D

For detail dimensions see IEC 191-2 (A50C)

CAUTION: THESE ARE STATIC SENSITIVE DEVICES - See clause 1.11**1. Limiting conditions of use (not for inspection purposes)**All voltages referenced to V_{SS}

1.1	Maximum supply voltage, positive	V_{DD}	+18,0 V
1.2	Maximum supply voltage, negative	V_{DD}	-0,5 V
1.3	Maximum positive input voltage	V_{IN}	$V_{DD} +0,5 V$
1.4	Maximum negative input voltage	V_{IN}	-0,5 V

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1. Limiting conditions of use (cont'd)

- | | | | |
|---------|--|-----------|-----------------------------------|
| 1.5 | Maximum power dissipation, per package | P_{D1} | 180 mW |
| | per output | P_{D2} | 30 mW |
| 1.6 | Maximum continuous current into any input. | $ I_I $ | 10,0 mA |
| 1.7 | Maximum continuous current into any output. | $ I_O $ | 10,0 mA |
| 1.8 | Operating temperature range | T_{amb} | |
| | | Full | -55 to +125 °C |
| | | Limited | -40 to + 85 °C |
| 1.9 | Storage temperature range | T_{stg} | -65 to +150 °C |
| 1.10 | Transient energy rating | | 400 V at 100 pF
through 1,5 kΩ |
| 1.11 | <u>Recommended handling precautions</u> | | |
| 1.11.1 | Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method. | | |
| 1.11.2 | Use grounded tip soldering irons. | | |
| 1.11.3 | Grounded all test equipment. | | |
| 1.11.4 | Connect all unused device inputs to V_{DD} or V_{SS} . | | |
| 1.11.5 | PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations. | | |
| 1.11.6 | Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices. | | |
| 1.11.7 | Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during inspection or handling. | | |
| 1.11.8 | When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage, 'Dummy connectors' should be used to electrically short all PC board terminals together. | | |
| 1.11.9 | Switch off power supply before inserting or removing devices from circuits. | | |
| 1.11.10 | Disconnect all low impedance equipment and input signals from the device before d.c. power supplies are switched off. | | |

2. Recommended conditions of use and associated characteristics (not for inspection purposes)

These apply over the operating temperature range unless otherwise stated. All voltages referenced to V_{SS} .

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} + 25 °C	T_{amb} HIGH	Unit
Quiescent device current (per package) CMOS-CMOS mode	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$						
Full temperature range	Outputs open circuit	I_{DDA}	5,0	0,05	0,05	1,5	μA
		I_{DDA}	10,0	0,10	0,10	3,0	μA
		I_{DDA}	15,0	0,20	0,20	6,0	μA
Limited temperature range		I_{DDA}	5,0	0,05	0,05	3,8	μA
		I_{DDA}	10,0	0,10	0,10	7,5	μA
		I_{DDA}	15,0	0,20	0,20	15,0	μA
Quiescent device current (per package) TTL - CMOS mode							
		I_{DDA}	5,0	0,50	0,50	3,80	μA
		I_{DDA}	10,0	1,00	1,00	7,50	μA
		I_{DDA}	15,0	2,00	2,00	15,0	μA
Quiescent device current (per package) TTL - CMOS mode							
		I_{CCA}	5,0	5,0	5,0	6,0	mA
		I_{CCA}	10,0	5,0	5,0	6,0	mA
		I_{CCA}	15,0	5,0	5,0	6,0	mA
LOW level output voltage at $ I_O < 1,0 \mu A$	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$						
		V_{OLA}	5,0	0,05	0,05	0,05	V
		V_{OLA}	10,0	0,05	0,05	0,05	V
		V_{OLA}	15,0	0,05	0,05	0,05	V
HIGH level output voltage at $ I_O < 1,0 \mu A$	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$						
		V_{OHB}	5,0	4,95	4,95	4,95	V
		V_{OHB}	10,0	9,95	9,95	9,95	V
		V_{OHB}	15,0	14,95	14,95	14,95	V
LOW level output voltage (for worst case combinations) at $ I_O < 1,0 \mu A$	$V_{IL} = 1,5 V$ $V_{IL} = 3,0 V$ $V_{IL} = 4,0 V$						
		V_{OLA}	5,0	0,5	0,5	0,5	V
		V_{OLA}	10,0	1,0	1,0	1,0	V
		V_{OLA}	15,0	1,5	1,5	1,5	V
HIGH level output voltage (for worst case combinations) at $ I_O < 1,0 \mu A$	$V_{IH} = 3,5 V$ $V_{IH} = 7,0 V$ $V_{IH} = 11,0 V$						
		V_{OHB}	5,0	4,5	4,5	4,5	V
		V_{OHB}	10,0	9,0	9,0	9,0	V
		V_{OHB}	15,0	13,5	13,5	13,5	V

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = +25 °C	T_{amb} HIGH	Unit
Output LOW (sink) current							
Full temperature range	$V_0 = 0,4 V$	I_{OLB}	5,0	0,64	0,51	0,36	mA
	$V_0 = 0,5 V$	I_{OLB}	10,0	1,60	1,30	0,90	mA
	$V_0 = 1,5 V$	I_{OLB}	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_0 = 0,4 V$	I_{OLB}	5,0	0,52	0,44	0,36	mA
	$V_0 = 0,5 V$	I_{OLB}	10,0	1,30	1,10	0,90	mA
	$V_0 = 1,5 V$	I_{OLB}	15,0	3,60	3,00	2,40	mA
Output HIGH (source) current							
Full temperature range	$V_0 = 4,6 V$	$-I_{OHB}$	5,0	0,64	0,51	0,36	mA
	$V_0 = 9,5 V$	$-I_{OHB}$	10,0	1,60	1,30	0,90	mA
	$V_0 = 13,5 V$	$-I_{OHB}$	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_0 = 4,6 V$	$-I_{OHB}$	5,0	0,52	0,44	0,36	mA
	$V_0 = 9,5 V$	$-I_{OHB}$	10,0	1,30	1,10	0,90	mA
	$V_0 = 13,5 V$	$-I_{OHB}$	15,0	3,60	3,00	2,40	mA
Input LOW level voltage							
TTL - CMOS	$V_0 = 1,0 V$	V_{ILA}	10,0	0,8	0,8	0,8	V
	$V_0 = 1,5 V$	V_{ILA}	15,0	0,8	0,8	0,8	V
CMOS - CMOS	$V_0 = 1,0 V$	V_{ILA}	10,0	1,5	1,5	1,4	V
	$V_0 = 1,5 V$	V_{ILA}	15,0	1,5	1,5	1,5	V
	$V_0 = 1,5 V$	V_{ILA}	15,0	3,0	3,0	2,9	V
Input HIGH level voltage							
TTL - CMOS	$V_0 = 9,0 V$	V_{IHB}	10,0	2,0	2,0	2,0	V
	$V_0 = 13,5 V$	V_{IHB}	15,0	2,0	2,0	2,0	V
CMOS - CMOS	$V_0 = 9,0 V$	V_{IHB}	10,0	3,6	3,5	3,5	V
	$V_0 = 13,5 V$	V_{IHB}	15,0	3,6	3,5	3,5	V
	$V_0 = 13,5 V$	V_{IHB}	15,0	7,1	7,0	7,0	V
Input leakage current	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$						
Full temperature range		$ I_{IA} $	15,0	0,10	0,10	1,00	μA
Limited temperature range		$ I_{IA} $	15,0	0,30	0,30	1,00	μA

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = +25 °C	T_{amb} HIGH	Unit
Input capacitance per unit load (Any input)	$V_I = 0 V$ $f = 1 MHz$	C_{IA}	-	-	7,5	-	pF
Noise margin at LOW level output (equal to the difference between V_{IL} and V_{OL} for worst case combinations)		V_{NLB} V_{NLB} V_{NLB}	5,0 10,0 15,0	1,0 2,0 2,5	1,0 2,0 2,5	1,0 2,0 2,5	V V V
Noise margin at HIGH level output (equal to the difference between V_{IH} and V_{OH} or worst case combinations)		V_{NHB} V_{NHB} V_{NHB}	5,0 10,0 15,0	1,0 2,0 2,5	1,0 2,0 2,5	1,0 2,0 2,5	V V V
Propagation and Transition Times	$C_L = 50 pF$ (Test conditions as in Sub-group A5)						
Propagation Delay Time LOW to HIGH level, TTL - CMOS $V_{DD} > V_{CC}$	$V_{CC} = 5,0 V$ $V_{CC} = 5,0 V$	t_{PLHA} t_{PLHA}	10,0 15,0	- -	340 320	- -	ns ns
CMOS - CMOS $V_{DD} > V_{CC}$	$V_{CC} = 5,0 V$ $V_{CC} = 5,0 V$ $V_{CC} = 10,0 V$	t_{PLHA} t_{PLHA} t_{PLHA}	10,0 15,0 15,0	- - -	340 340 200	- - -	ns ns ns
CMOS - CMOS $V_{CC} > V_{DD}$	$V_{CC} = 10,0 V$ $V_{CC} = 15,0 V$ $V_{CC} = 15,0 V$	t_{PLHA} t_{PLHA} t_{PLHA}	5,0 5,0 10,0	- - -	550 550 290	- - -	ns ns ns
Propagation Delay Time HIGH to LOW level TTL - CMOS $V_{DD} > V_{CC}$	$V_{CC} = 5,0 V$ $V_{CC} = 5,0 V$	t_{PHLA} t_{PHLA}	10,0 15,0	- -	280 280	- -	ns ns
CMOS - CMOS $V_{DD} > V_{CC}$	$V_{CC} = 5,0 V$ $V_{CC} = 5,0 V$ $V_{CC} = 10,0 V$	t_{PHLA} t_{PHLA} t_{PHLA}	10,0 15,0 15,0	- - -	240 240 140	- - -	ns ns ns

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25°C	T _{amb} HIGH	Unit
Propagation Delay Time (cont'd) CMOS - CMOS V _{CC} > V _{DD}	V _{CC} = 10,0 V	t _{PHLA}	5,0	-	370	-	ns
	V _{CC} = 15,0 V	t _{PHLA}	5,0	-	370	-	ns
	V _{CC} = 15,0 V	t _{PHLA}	10,0	-	-	-	ns
Transition Time LOW to HIGH and HIGH to LOW level.		t _{TLHA} / t _{THLA}	5,0	-	200,0	-	ns
		t _{TLHA} / t _{THLA}	10,0	-	100,0	-	ns
		t _{TLHA} / t _{THLA}	15,0	-	80,0	-	ns

Table 1
(Function Truth Table)

INPUT	MODE	OUTPUT	MODE
H	V _{CC}	H	TTL
L	V _{CC}	L	TTL
H	V _{SS}	H	CMOS
L	V _{SS}	L	CMOS

H = High level

L = Low level

Terminal Identification

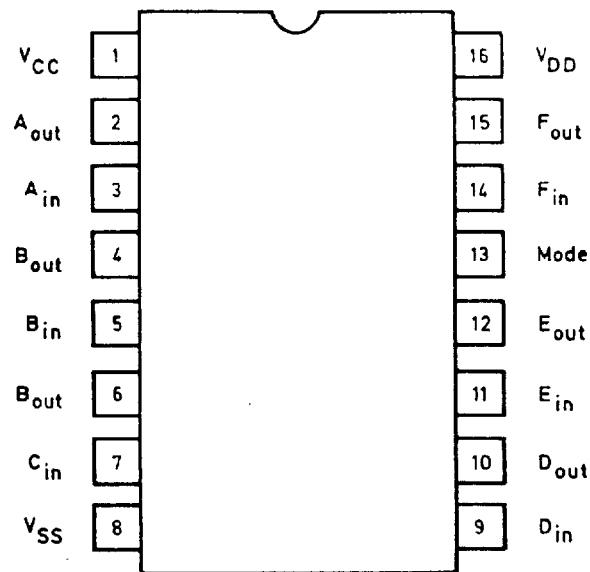


Figure 1

Logic Diagram

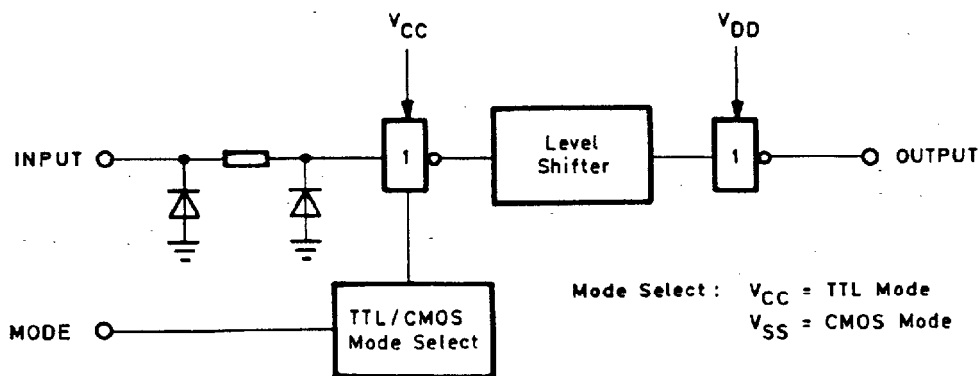


Figure 2

Input Switchpoint CMOS to CMOS mode

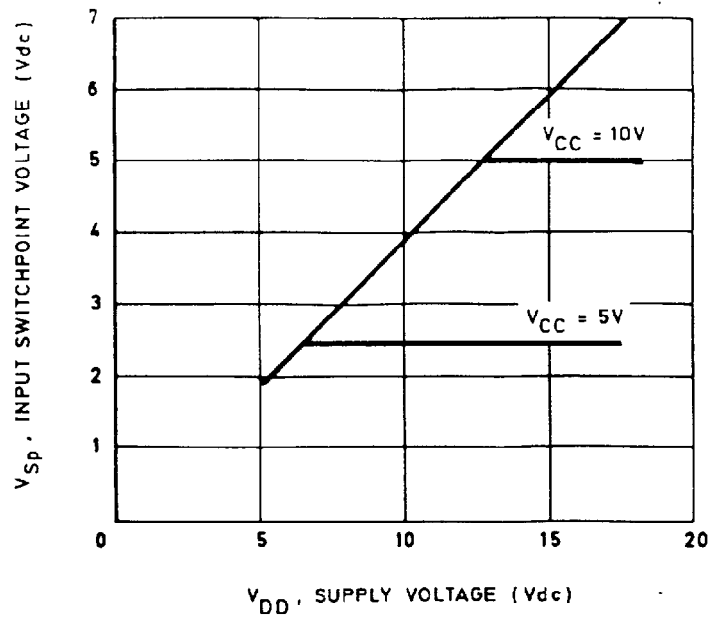


Figure 3

Input Switchpoint TTL to CMOS mode

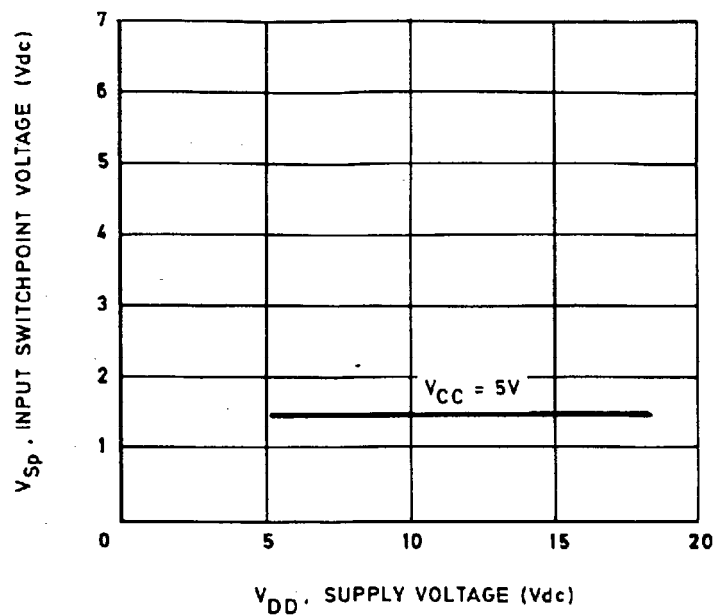


Figure 4

Operating Boundary CMOS to CMOS mode

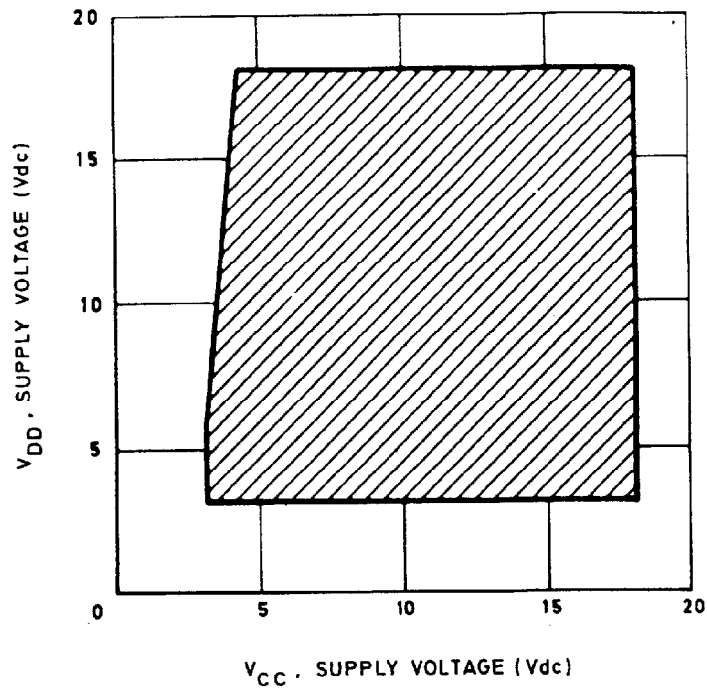


Figure 5

Operating Boundary TTL to CMOS mode

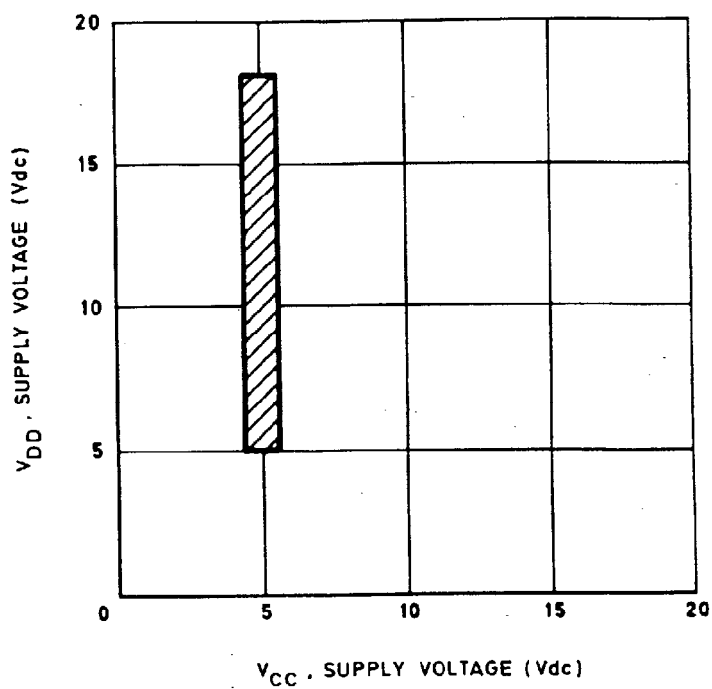


Figure 6