

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON, W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 ANDMOTOROLA LTD,
KELVIN ESTATE,
EAST KILBRIDE.
G75 OTG

BS CECC 90 104-217

ISSUE 1

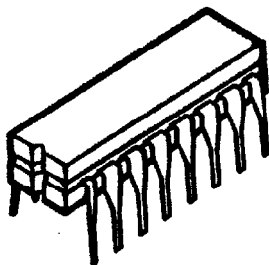
MARCH 1985



Page 1 of 30 pages

ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:BS CECC 90 000 : 1982
BS CECC 90 100 : 1983

MANUFACTURERS TYPE NUMBER

4530BSEE PD 9002 AND CECC 00 200
For ordering information
see pageOutline not to scale: Isometric projection
Marking information see page 12DUAL 5-INPUT MAJORITY LOGIC
GATESILICON COMPLEMENTARY MOS.
WITH (B) BUFFERED OUTPUTS AND
CAVITY PACKAGING.Assessment levels
R, T and V
and optional screening
categories A, B, C and D

For detail dimensions see IEC 191-2 (A50C)

CAUTION: THESE ARE STATIC SENSITIVE DEVICES - See clause 1.11**Limiting conditions of use (not for inspection purposes)**All voltages referenced to V_{SS}

1.1	Maximum supply voltage, positive	V_{DD}	+18,0 V
1.2	Maximum supply voltage, negative	V_{DD}	-0,5 V
1.3	Maximum positive input voltage	V_{IN}	$V_{DD} + 0,5 V$
1.4	Maximum negative input voltage	V_{IN}	-0,5 V

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

- 1 -

BS CECC 90 104-217
Issue 1

1. Limiting conditions of use (cont'd)

1.5	Maximum power dissipation, per package	P_{D1}	136 mW
	per output	P_{D2}	68 mW
1.6	Maximum continuous current into any input.	$ I_I $	10,0 mA
1.7	Maximum continuous current into any output.	$ I_O $	10,0 mA
1.8	Operating temperature range	T_{amb}	
		Full	-55 to +125 °C
		Limited	-40 to + 85 °C
1.9	Storage temperature range	T_{stg}	-65 to +150 °C
1.10	Transient energy rating		400 V at 100 pF through 1,5 kΩ

1.11 Recommended handling precautions

- 1.11.1 Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method.
- 1.11.2 Use grounded tip soldering irons.
- 1.11.3 Ground all test equipment.
- 1.11.4 Connect all unused device inputs to V_{DD} or V_{SS} .
- 1.11.5 PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations.
- 1.11.6 Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices.
- 1.11.7 Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during inspection or handling.
- 1.11.8 When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage, 'Dummy connectors' should be used to electrically short all PC board terminals together.
- 1.11.9 Switch off power supply before inserting or removing devices from circuits.
- 1.11.10 Disconnect all low impedance equipment and input signals from the device before d.c. power supplies are switched off.

2. Recommended conditions of use and associated characteristics (not for inspection purposes)

These apply over the operating temperature range unless otherwise stated. All voltages referenced to V_{SS} .

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = +25 °C	T_{amb} HIGH	Unit
Quiescent device current	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$						
Full temperature range	Outputs open circuit	I_{DDA}	5,0	0,25	0,25	7,5	μA
		I_{DDA}	10,0	0,50	0,50	15,0	μA
		I_{DDA}	15,0	1,00	1,00	30,0	μA
Limited temperature range		I_{DDA}	5,0	1,00	1,00	7,5	μA
		I_{DDA}	10,0	2,00	2,00	15,0	μA
		I_{DDA}	15,0	4,00	4,00	30,0	μA
LOW level output voltage at $ I_O < 1,0 \mu A$	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$	V_{OLA}	5,0	0,05	0,05	0,05	V
		V_{OLA}	10,0	0,05	0,05	0,05	V
		V_{OLA}	15,0	0,05	0,05	0,05	V
HIGH level output voltage at $ I_O < 1,0 \mu A$	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$	V_{OHB}	4,0	4,95	4,95	4,95	V
		V_{OHB}	10,0	9,95	9,95	9,95	V
		V_{OHB}	15,0	14,95	14,95	14,95	V
LOW level input voltage		V_{ILA}	5,0	1,2	1,25	1,15	V
		V_{ILA}	10,0	2,5	2,5	2,40	V
		V_{ILA}	15,0	3,0	3,0	2,90	V
HIGH level input voltage		V_{IHB}	5,0	3,85	3,75	3,75	V
		V_{IHB}	10,0	7,6	7,5	7,5	V
		V_{IHB}	15,0	12,1	12,0	12,0	V
Output LOW (sink) current							
Full temperature range	$V_O = 0,4 V$	I_{OLB}	5,0	0,64	0,51	0,36	mA
	$V_O = 0,5 V$	I_{OLB}	10,0	1,60	1,30	0,90	mA
	$V_O = 1,5 V$	I_{OLB}	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_O = 0,4 V$	I_{OLB}	5,0	0,52	0,44	0,36	mA
	$V_O = 0,5 V$	I_{OLB}	10,0	1,30	1,10	0,90	mA
	$V_O = 1,5 V$	I_{OLB}	15,0	3,60	3,00	2,40	mA

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = +25 °C	T _{amb} HIGH	Unit
Output HIGH (source) current							
Full temperature range	V _O = 4,6 V	-I _{OHB}	5,0	0,64	0,51	0,36	mA
	V _O = 9,5 V	-I _{OHB}	10,0	1,60	1,30	0,90	mA
	V _O = 13,5 V	-I _{OHB}	15,0	4,20	3,40	2,40	mA
Limited temperature range	V _O = 4,6 V	-I _{OHB}	5,0	0,52	0,44	0,36	mA
	V _O = 9,5 V	-I _{OHB}	10,0	1,30	1,10	0,90	mA
	V _O = 13,5 V	-I _{OHB}	15,0	3,60	3,00	2,40	mA
Input leakage Current	V _{IL} = 0 V V _{IH} = V _{DD}						
Full temperature range		I _{IA}	15,0	0,10	0,10	1,00	μA
Limited temperature range		I _{IA}	15,0	0,30	0,30	1,00	μA
Input capacitance per unit load (Any input)	V _I = 0 V f = 1 MHz	C _{IA}	-	-	7,5	-	pF
Noise margin at LOW level output (equal to the difference between V _{IL} and V _{OL} for worst case combinations)		V _{NLB}	5,0	1,0	1,0	1,0	V
		V _{NLB}	10,0	2,0	2,0	2,0	V
		V _{NLB}	15,0	2,5	2,5	2,5	V
Noise margin at HIGH level output (equal to the difference between V _{IH} and V _{OH} for worst case combinations)		V _{NHB}	5,0	1,0	1,0	1,0	V
		V _{NHB}	10,0	2,0	2,0	2,0	V
		V _{NHB}	15,0	2,5	2,5	2,5	V
Propagation and Transition Times	C _L = 50 pF (Test conditions as in Sub-group A5)						

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = +25 °C	T _{amb} HIGH	Unit
Propagation Delay Time, LOW to HIGH and HIGH to LOW level A, C, W = V _{DD} ; B, E = Gnd; D = Pulse Generator		t _{PLHA}	5,0	-	960,0	-	ns
		t _{PLHA}	10,0	-	400,0	-	ns
		t _{PLHA}	15,0	-	300,0	-	ns
		t _{PHLA}	5,0	-	1200,0	-	ns
		t _{PHLA}	10,0	-	540,0	-	ns
		t _{PHLA}	15,0	-	410,0	-	ns
Propagation Delay Time, LOW to HIGH and HIGH to LOW level A, B, C, D, E = Pulse Generator; W = V _{DD}		t _{PLHA}	5,0	-	640,0	-	ns
		t _{PLHA}	10,0	-	300,0	-	ns
		t _{PLHA}	15,0	-	210,0	-	ns
		t _{PHLA}	5,0	-	750,0	-	ns
		t _{PHLA}	10,0	-	330,0	-	ns
		t _{PHLA}	15,0	-	250,0	-	ns
Propagation Delay Time, LOW to HIGH and HIGH TO LOW level A, B, C, D, E = Gnd; W = Pulse Generator		t _{PLHA} /	5,0	-	575,0	-	ns
		t _{PHLA}	10,0	-	265,0	-	ns
			15,0	-	190,0	-	ns
Transition Time LOW to HIGH and HIGH to LOW level		t _{TLHA} /	5,0	-	200,0	-	ns
		t _{THLA}	10,0	-	100,0	-	ns
			15,0	-	80,0	-	ns

Terminal identification

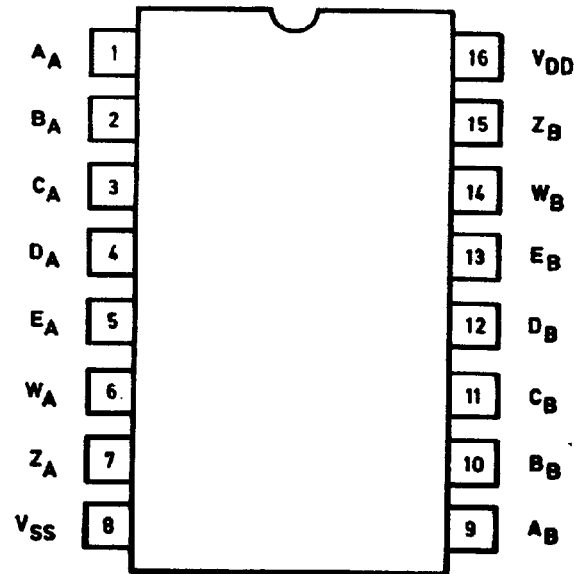


Figure 1

Function Table

Table 1

M ₅	W	Z
L	L	H
L	H	L
H	L	L
H	H	H

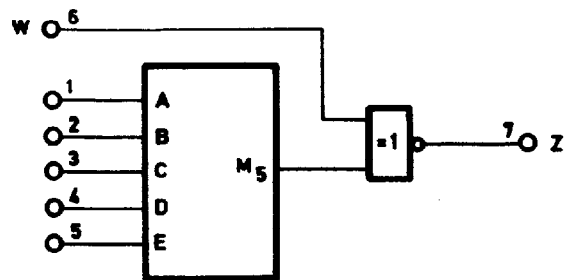
V_{DD} = Pin 16

V_{SS} = Pin 8

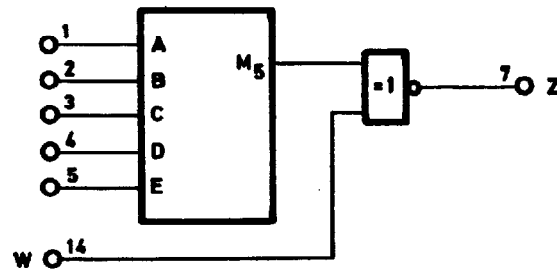
H = HIGH level

L = LOW level

Logic diagrams



$$Z = M_5 \odot W = (ABC+ABD+ABE+ACD+ACE+ADE+BCD+BCE+BDE+CDE) \odot W$$



* M_5 is a logical "H" if any three or more inputs are logical "H"s.

$\odot \equiv \text{Exclusive NOR} \equiv \overline{\text{Exclusive OR}}$

This is a graphic representation not a circuit diagram

Figure 2

Power Dissipation Test Circuit and Waveform

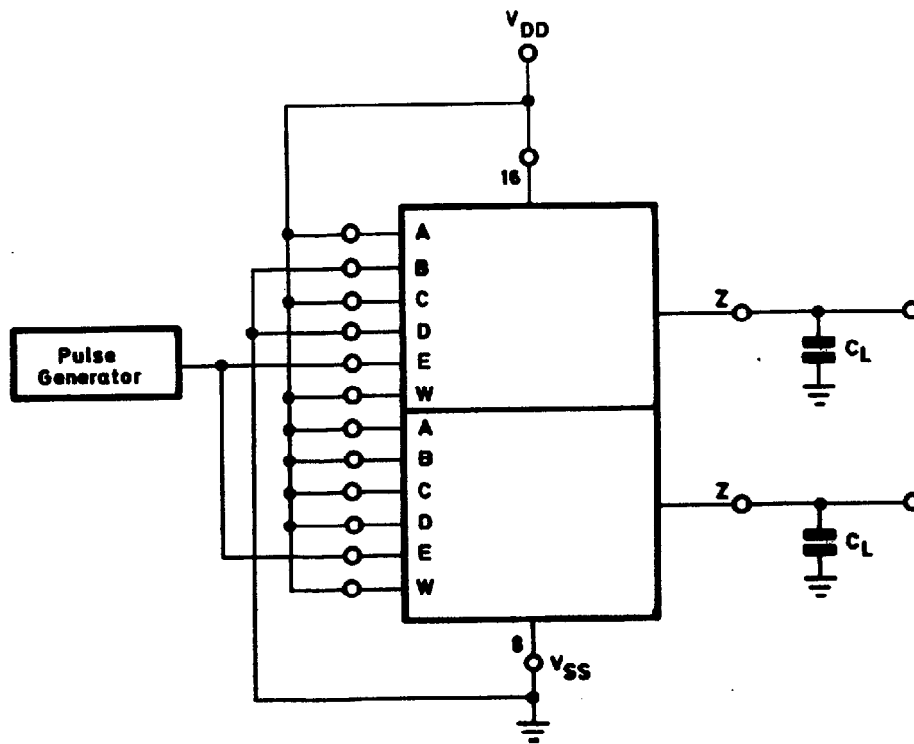


Figure 3a

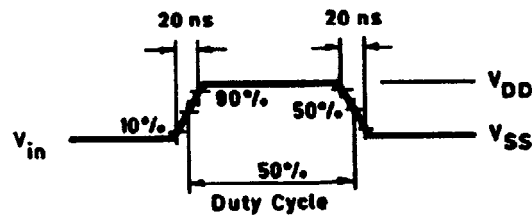


Figure 3b

Sequential Logic Applications

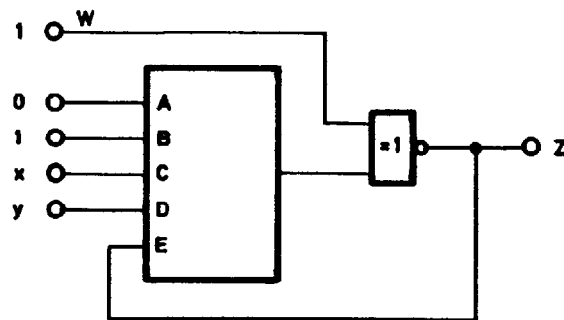


Figure 4

Coincident Flip-Flop

Table 2

X	Y	$Q_n + 1$
L	L	L
L	H	Q
H	L	Q
H	H	H

A flip-flop that will change only when both inputs agree.

H = HIGH level
L = LOW level