

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON, W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 ANDMOTOROLA LTD,
KELVIN ESTATE,
EAST KILBRIDE.
G75 OTG

BS CECC 90 104 - 218

ISSUE 1

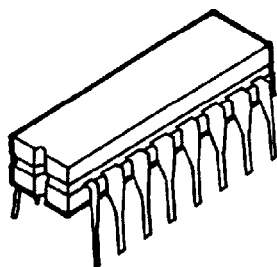
AUGUST 1985



Page 1 of 37 pages

ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:BS CECC 90 000 : 1982
BS CECC 90 100 : 1983

MANUFACTURERS TYPE NUMBER

4536BSEE PD 9002 AND CECC 00 200
For ordering information
see page 16Outline not to scale: Isometric projection
Marking information see page 15

PROGRAMMABLE TIMER

SILICON COMPLEMENTARY MOS.
WITH (B) BUFFERED OUTPUTS AND
CAVITY PACKAGING.Assessment levels
R, T and V
and optional screening
categories A, B, C and D

For detail dimensions see IEC 191-2 (A50C)

CAUTION: THESE ARE STATIC SENSITIVE DEVICES - See clause 1.11Limiting conditions of use (not for inspection purposes)All voltages referenced to V_{SS}

1.1	Maximum supply voltage, positive	V_{DD}	+18,0 V
1.2	Maximum supply voltage, negative	V_{DD}	-0,5 V
1.3	Maximum positive input voltage	V_{IN}	$V_{DD} + 0,5 V$
1.4	Maximum negative input voltage	V_{IN}	-0,5 V

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1. Limiting conditions of use (contd)

1.5	Maximum power dissipation, per package	P_{D1}	347 mW
	per output	P_{D2}	116 mW
1.6	Maximum continuous current into any input.	$ I_I $	10,0 mA
1.7	Maximum continuous current into any output.	$ I_O $	10,0 mA
1.8	Operating temperature range	T_{amb}	
		Full	-55 to +125 °C
		Limited	-40 to + 85 °C
1.9	Storage temperature range	T_{stg}	-65 to +150 °C
1.10	Transient energy rating		400 V at 100 pF through 1,5 kΩ
1.11	<u>Recommended handling precautions</u>		
1.11.1	Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method.		
1.11.2	Use grounded tip soldering irons.		
1.11.3	Ground all test equipment.		
1.11.4	Connect all unused device inputs to V_{DD} or V_{SS} .		
1.11.5	PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations.		
1.11.6	Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices.		
1.11.7	Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during inspection or handling.		
1.11.8	When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage, 'Dummy connectors' should be used to electrically short all PC board terminals together.		
1.11.9	Switch off power supply before inserting or removing devices from circuits.		
1.11.10	Disconnect all low impedance equipment and input signals from the device before d.c. power supplies are switched off.		

2. Recommended conditions of use and associated characteristics (not for inspection purposes)

These apply over the operating temperature range unless otherwise stated. All voltages referenced to V_{SS} .

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25 °C	T_{amb} HIGH	Unit
Quiescent device current	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$						
Full temperature range	Outputs open circuit	I_{DDA}	5,0	5,0	5,0	150,0	μA
		I_{DDA}	10,0	10,0	10,0	300,0	μA
		I_{DDA}	15,0	20,0	20,0	600,0	μA
Limited temperature range		I_{DDA}	5,0	50,0	50,0	375,0	μA
		I_{DDA}	10,0	100,0	100,0	750,0	μA
		I_{DDA}	15,0	200,0	200,0	1500,0	μA
LOW level output voltage at $ I_O < 1,0 \mu A$	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$	V_{OLA}	5,0	0,05	0,05	0,05	V
		V_{OLA}	10,0	0,05	0,05	0,05	V
		V_{OLA}	15,0	0,05	0,05	0,05	V
HIGH level output voltage at $ I_O < 1,0 \mu A$	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$	V_{OHB}	5,0	4,95	4,95	4,95	V
		V_{OHB}	10,0	9,95	9,95	9,95	V
		V_{OHB}	15,0	14,95	14,95	14,95	V
LOW level output voltage (for worst case combinations) at $ I_O < 1,0 \mu A$	$V_{IL} = 1,5 V$ $V_{IL} = 3,0 V$ $V_{IL} = 4,0 V$	V_{OLA}	5,0	0,5	0,5	0,5	V
		V_{OLA}	10,0	1,0	1,0	1,0	V
		V_{OLA}	15,0	1,5	1,5	1,5	V
HIGH level output voltage (for worst case combinations) at $ I_O < 1,0 \mu A$	$V_{IH} = 3,5 V$ $V_{IH} = 7,0 V$ $V_{IH} = 11,0 V$	V_{OHB}	5,0	4,5	4,5	4,5	V
		V_{OHB}	10,0	9,0	9,0	9,0	V
		V_{OHB}	15,0	13,5	13,5	13,5	V
Output LOW (sink) current							
Full temperature range	$V_O = 0,4 V$	I_{OLB}	5,0	0,64	0,51	0,36	mA
	$V_O = 0,5 V$	I_{OLB}	10,0	1,60	1,30	0,90	mA
	$V_O = 1,5 V$	I_{OLB}	15,0	4,20	3,40	2,40	mA

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Output LOW (sink) current (contd)							
Limited temperature range	$V_O = 0,4 V$	I_{OLB}	5,0	0,52	0,44	0,36	mA
	$V_O = 0,5 V$	I_{OLB}	10,0	1,30	1,10	0,90	mA
	$V_O = 1,5 V$	I_{OLB}	15,0	3,60	3,00	2,40	mA
Output HIGH (source) current (Pins 4 & 5)							
Full temperature range	$V_O = 4,6 V$	$-I_{OHB}$	5,0	0,25	0,20	0,14	mA
	$V_O = 9,5 V$	$-I_{OHB}$	10,0	0,62	0,50	0,35	mA
	$V_O = 13,5 V$	$-I_{OHB}$	15,0	1,80	1,50	1,10	mA
Limited temperature range	$V_O = 4,6 V$	$-I_{OHB}$	5,0	0,20	0,16	0,12	mA
	$V_O = 9,5 V$	$-I_{OHB}$	10,0	0,50	0,40	0,30	mA
	$V_O = 13,5 V$	$-I_{OHB}$	15,0	1,40	1,20	1,00	mA
Output HIGH (source) current (Pin 13)							
Full temperature range	$V_O = 4,6 V$	$-I_{OHB}$	5,0	0,64	0,51	0,36	mA
	$V_O = 9,5 V$	$-I_{OHB}$	10,0	1,60	1,30	0,90	mA
	$V_O = 13,5 V$	$-I_{OHB}$	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_O = 4,6 V$	$-I_{OHB}$	5,0	0,52	0,44	0,36	mA
	$V_O = 9,5 V$	$-I_{OHB}$	10,0	1,30	1,10	0,90	mA
	$V_O = 13,5 V$	$-I_{OHB}$	15,0	3,60	3,00	2,40	mA
Input leakage current	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$						
Full temperature range		$ I_{IA} $	15,0	0,10	0,10	1,00	μA
Limited temperature range		$ I_{IA} $	15,0	0,30	0,30	1,00	μA
Input capacitance per unit load (Any input)	$V_I = 0 V$ $f = 1 MHz$	C_{IA}	-	-	7,5	-	pF

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25 °C	T _{amb} HIGH	Unit
Noise margin at LOW level output (equal to the difference between V _{IL} and V _{OL} for worst case combinations)		V _{NLB}	5,0	1,0	1,0	1,0	V
		V _{NLB}	10,0	2,0	2,0	2,0	V
		V _{NLB}	15,0	2,5	2,5	2,5	V
Noise margin at HIGH level output (equal to the difference between V _{IH} and V _{OH} for worst case combinations)		V _{NHB}	5,0	1,0	1,0	1,0	V
		V _{NHB}	10,0	2,0	2,0	2,0	V
		V _{NHB}	15,0	2,5	2,5	2,5	V
Propagation and Transition Times	C _L = 50 pF (Test conditions as in Sub-group A5)						
Propagation Delay Time LOW to HIGH and HIGH to LOW level Clock to Output (Q1) 8-Bypass (Pin 6) HIGH. Binary Select A,B,C,D Low.		t _{PLHA} /	5,0	-	3600,0	-	ns
		t _{PHLA}	10,0	-	1300,0	-	ns
			15,0	-	1000,0	-	ns
Propagation Delay Time LOW to HIGH and HIGH to LOW level Clock to Output (Q1), 8-Bypass (Pin 6) low. Output (Q9), A,B,C,D Low.		t _{PLHA} /	5,0	-	7,6	-	µs
		t _{PHLA}	10,0	-	3,0	-	µs
			15,0	-	2,3	-	µs
Propagation Delay Time LOW to HIGH and HIGH to LOW level Clock to Output (Q16), 8-Bypass HIGH and A,B,C,D HIGH		t _{PLHA} /	5,0	-	14,0	-	µs
		t _{PHLA} /	10,0	-	6,0	-	µs
			15,0	-	4,5	-	µs
Propagation Delay Time HIGH to LOW level Reset to Qn		t _{PHLA}	5,0	-	3000,0	-	ns
			10,0	-	1200,0	-	ns
			15,0	-	900,0	-	ns

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25 °C	T _{amb} HIGH	Unit
Transition Time (Counter Outputs) LOW to HIGH and HIGH to LOW level		t _{TLHA} / t _{THLA}	5,0	-	200,0	-	ns
			10,0	-	100,0	-	ns
			15,0	-	80,0	-	ns
Clock Pulse Width		t _{PWCB}	5,0	-	600,0	-	ns
			10,0	-	200,0	-	ns
			15,0	-	170,0	-	ns
Clock Pulse Frequency (50 % Duty Cycle)		f _{max.A}	5,0	-	0,4	-	MHz
			10,0	-	1,5	-	MHz
			15,0	-	2,0	-	MHz
Clock Rise and Fall Time		t _{rA} / t _{fA}	5,0	NO LIMIT			
			10,0				
			15,0				
Reset Pulse Width		t _{PWRB}	5,0	-	1000,0	-	ns
			10,0	-	400,0	-	ns
			15,0	-	300,0	-	ns
Total Supply Current		I _T	5,0	I _T =(1,15µA/kHz) f+I _{DD}			µA
			10,0	I _T =(2,3µA/kHz) f+I _{DD}			µA
			15,0	I _T =(3,55µA/kHz) f+I _{DD}			µA

Terminal identification

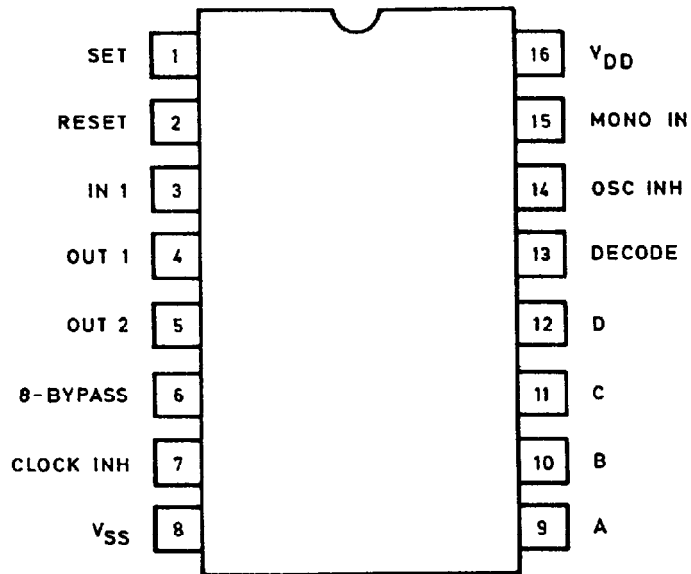


Figure 1

Function Table

Table 1

IN ₁	Set	Reset	Clock Inh	Osc Inh	Out 1	Out 2	Decode Out
$\nearrow$	L	L	L	L	$\nearrow$	$\searrow$	No Change
$\searrow$	L	L	L	L	$\searrow$	$\nearrow$	Advance to next state
X	H	L	L	L	L	H	H
X	L	H	L	L	L	H	L
X	L	L	H	L			No Change
L	L	L	L	X	L	H	No Change
H	L	L	L	$\nearrow$	$\searrow$	$\nearrow$	Advance to next state

H = High level
 L = Low level
 X = Level irrelevant
 $\nearrow$ = Transition from low to high
 $\searrow$ = Transition from high to low

Truth Table

Table 2

D	C	B	A	8-Bypass	
				L	H
L	L	L	L	9	1
L	L	L	H	10	2
L	L	H	L	11	3
L	L	H	H	12	4
L	H	L	L	13	5
L	H	L	H	14	6
L	H	H	L	15	7
L	H	H	H	16	8
H	L	L	L	17	9
H	L	L	H	18	10
H	L	H	L	19	11
H	L	H	H	20	12
H	H	L	L	21	13
H	H	L	H	22	14
H	H	H	L	23	15
H	H	H	H	24	16

- 8 -

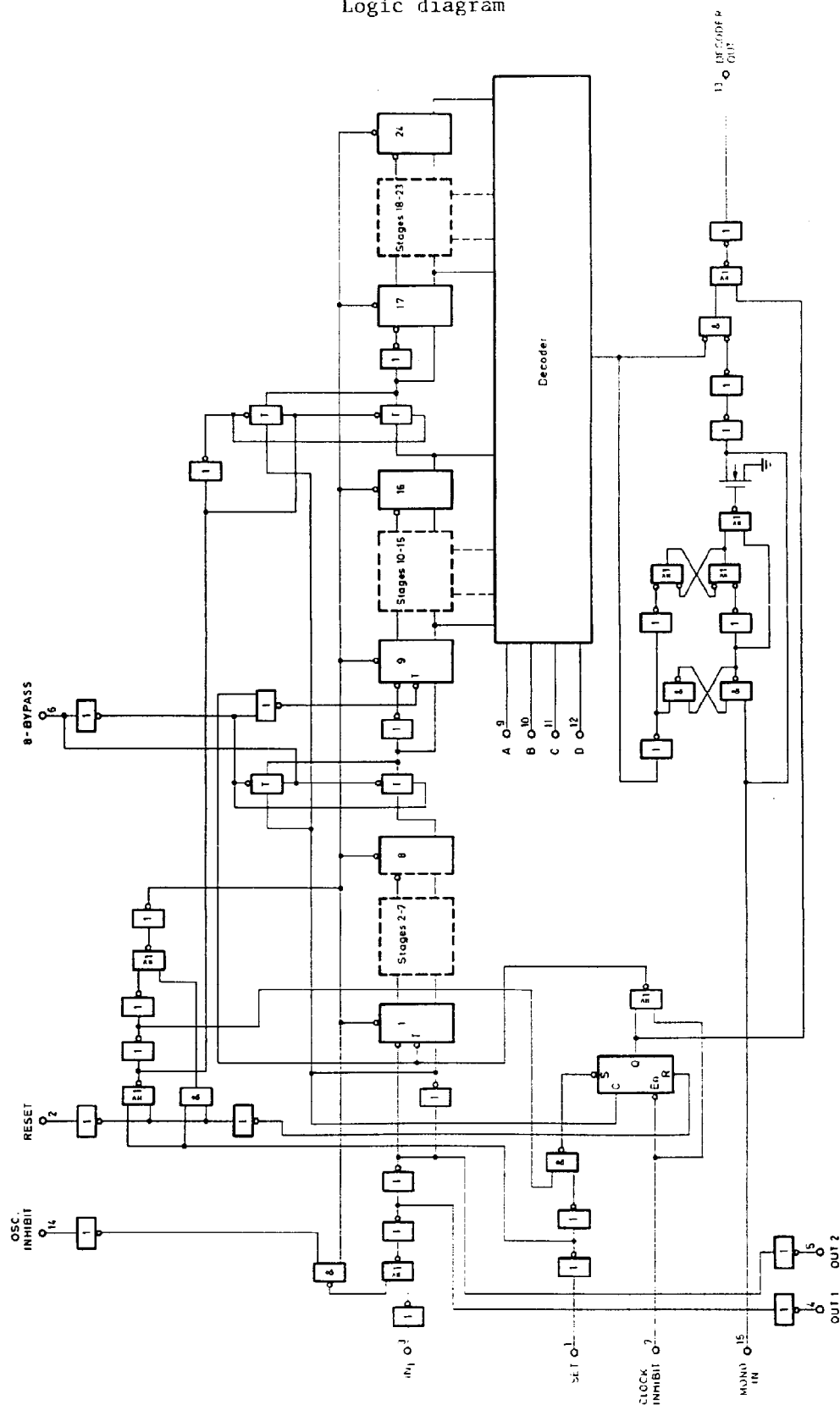
BS CECC 90 104 - 218
Issue 1



Documents

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Logic diagram



This is a graphic representation, not a circuit diagram

Figure 2

Switching Time Waveform

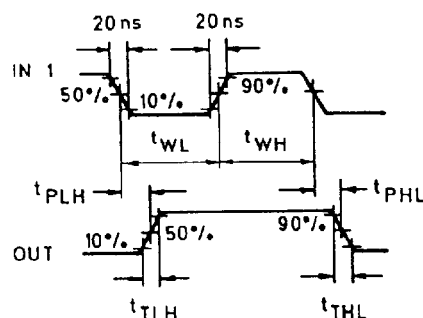


Figure 3

GENERAL

Operating Characteristics

Set input initializes output to a "H". This is accomplished by setting an output conditioning latch to a H while at the same time resetting the 24 flip-flop stages. With the occurrence of the first negative transition of the clock, the output will change to a "L". When the circuit is in the Set condition, the counter flip-flop stages will start counting on the second negative transition. The resulting behaviour is the same as if each of the 24 flip-flop stages were set.

Reset inputs resets all stages to a logical "L". Reset or Set also disables the on-chip RC oscillator to allow very low power standby operation. In₁ input is used as the external Clock input or as the input to the on-chip RC oscillator.

Out 1, Out 2 outputs are used in the on-chip RC oscillator configuration.

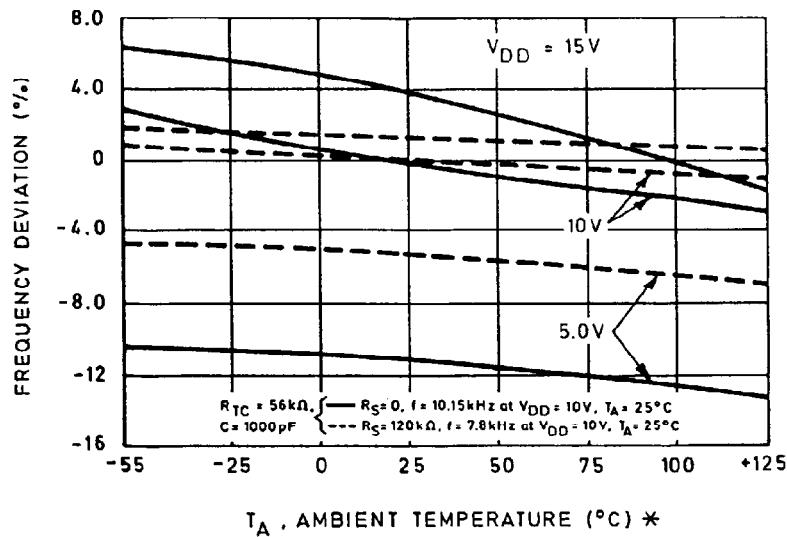
8-Bypass input bypasses the first eight stages resulting in a 16-stage counter with all 16 stages selectable, one at a time. Clock Inhibit input disconnects the first counter stage from the input circuit, therefore inhibiting counting. This Clock Inhibit input is independent of the state of the Clock input. When the Clock Inhibit input is disabled, the counter will start counting only with the occurrence of the first negative edge of the Clock.

Binary Select inputs A, B, C, and D select the flip-flop stage to be connected to the output. Decode Out output can either be connected directly to a flip-flop output or to the monostable output. Osc Inhibit input can be used to disable the on-chip RC oscillator to allow very low power standby operation. Mono In input is used as the timing pin for the on-chip monostable oscillator. If the Mono In input is grounded through a resistor, the monostable circuit is disabled and the output is connected directly to the selected flip-flop. The monostable circuit is enabled if a resistor is connected between this pin and V_{DD} and a capacitor connected between this pin and ground. Any desired pulse width can be achieved depending upon the value of the R and C selected.

The test mode configuration divides the 24 flip-flop stages into three 8-stage sections to facilitate a fast test sequence. This test mode is enabled when 8-Bypass, Set and Reset are at a "H".

Typical RC Oscillator Characteristics

RC Oscillator stability



* Device only

Figure 4

RC Oscillator frequency as a function of R_{TC} and C

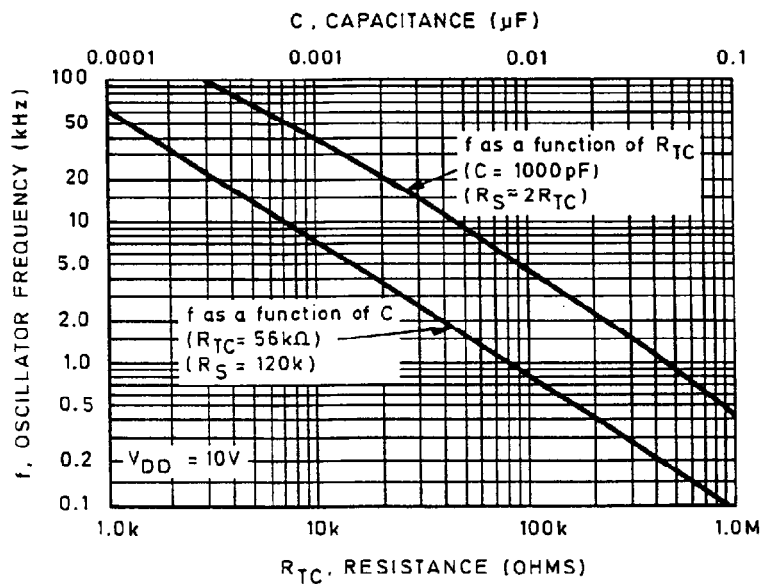


Figure 5

Monostable Characteristics

Typical C_X versus pulse width @ $V_{DD} = 5,0 \text{ V}$

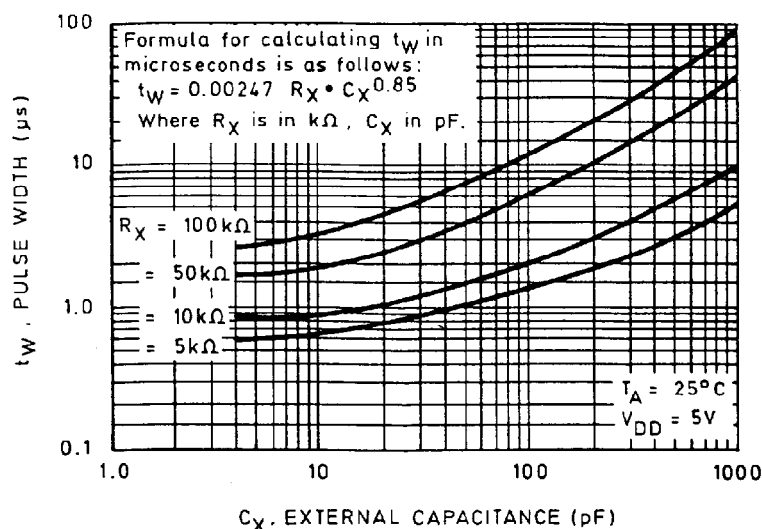


Figure 6

Typical C_X versus pulse width @ $V_{DD} = 10 \text{ V}$

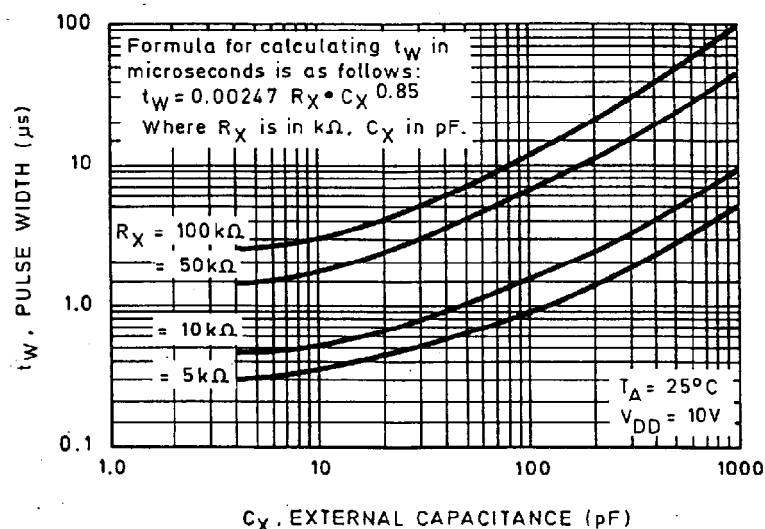


Figure 7