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BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON, W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 AND

MOTOROLA LTD,
KELVIN ESTATE,
EAST KILBRIDE.
G75 OTG

BS CECC 90 104 - 220

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ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:

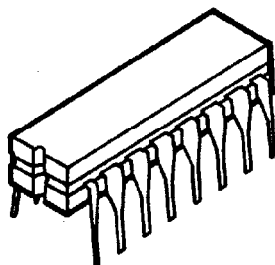
BS CECC 90 000 : 1982
BS CECC 90 100 : 1983

MANUFACTURERS TYPE NUMBER

4543B

SEE PD 9002 AND CECC 00 200
For ordering information
see page 12

Outline not to scale: Isometric projection
Marking information see page 12



BCD-TO-SEVEN SEGMENT
LATCH/DECODER/DRIVER
FOR LIQUID CRYSTALS

SILICON COMPLEMENTARY MOS.
WITH (B) BUFFERED OUTPUTS AND
CAVITY PACKAGING.

Assessment levels
R, T and V
and optional screening
categories A, B, C and D

For detail dimensions see IEC 191-2 (A50C)

CAUTION: THESE ARE STATIC SENSITIVE DEVICES - See clause 1.11

Limiting conditions of use (not for inspection purposes)

All voltages referenced to V_{SS}

1.1	Maximum supply voltage, positive	V_{DD}	+18,0 V
1.2	Maximum supply voltage, negative	V_{DD}	-0,5 V
1.3	Maximum positive input voltage	V_{IN}	$V_{DD} + 0,5 V$
1.4	Maximum negative input voltage	V_{IN}	-0,5 V

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1. Limiting conditions of use (contd)

1.5	Maximum power dissipation, per package	P_{D1}	945 mW
	per output	P_{D2}	135 mW
1.6	Maximum continuous current into any input.	$ I_I $	10,0 mA
1.7	Maximum continuous current into any output.	$ I_O $	10,0 mA
1.8	Operating temperature range	T_{amb}	
		Full	-55 to +125 °C
		Limited	-40 to + 85 °C
1.9	Storage temperature range	T_{stg}	-65 to +150 °C
1.10	Transient energy rating		400 V at 100 pF through 1,5 kΩ

1.11 Recommended handling precautions

- 1.11.1 Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method.
- 1.11.2 Use grounded tip soldering irons.
- 1.11.3 Ground all test equipment.
- 1.11.4 Connect all unused device inputs to V_{DD} or V_{SS} .
- 1.11.5 PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations.
- 1.11.6 Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices.
- 1.11.7 Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during inspection or handling.
- 1.11.8 When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage, 'Dummy connectors' should be used to electrically short all PC board terminals together.
- 1.11.9 Switch off power supply before inserting or removing devices from circuits.
- 1.11.10 Disconnect all low impedance equipment and input signals from the device before d.c. power supplies are switched off.

2. Recommended conditions of use and associated characteristics (not for inspection purposes)

These apply over the operating temperature range unless otherwise stated. All voltages referenced to V_{SS} .

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25 °C	T_{amb} HIGH	Unit
Quiescent device current	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$						
Full temperature range	Outputs open circuit	I_{DDA}	5,0	0,25	0,25	7,5	μA
		I_{DDA}	10,0	0,50	0,50	15,0	μA
		I_{DDA}	15,0	1,00	1,00	30,0	μA
Limited temperature range		I_{DDA}	5,0	1,0	1,0	7,5	μA
		I_{DDA}	10,0	2,0	2,0	15,0	μA
		I_{DDA}	15,0	4,0	4,0	30,0	μA
LOW level output voltage at $ I_O < 1,0 \mu A$	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$	V_{OLA}	5,0	0,05	0,05	0,05	V
		V_{OLA}	10,0	0,05	0,05	0,05	V
		V_{OLA}	15,0	0,05	0,05	0,05	V
HIGH level output voltage at $ I_O < 1,0 \mu A$	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$	V_{OHB}	5,0	4,95	4,95	4,95	V
		V_{OHB}	10,0	9,95	9,95	9,95	V
		V_{OHB}	15,0	14,95	14,95	14,95	V
LOW level output voltage (for worst case combinations) at $ I_O < 1,0 \mu A$	$V_{IL} = 1,5 V$ $V_{IL} = 3,0 V$ $V_{IL} = 4,0 V$	V_{OLA}	5,0	0,5	0,5	0,5	V
		V_{OLA}	10,0	1,0	1,0	1,0	V
		V_{OLA}	15,0	1,5	1,5	1,5	V
HIGH level output voltage (for worst case combinations) at $ I_O < 1,0 \mu A$	$V_{IH} = 3,5 V$ $V_{IH} = 7,0 V$ $V_{IH} = 11,0 V$	V_{OHB}	5,0	4,5	4,5	4,5	V
		V_{OHB}	10,0	9,0	9,0	9,0	V
		V_{OHB}	15,0	13,5	13,5	13,5	V
Output LOW (sink) current							
Full temperature range	$V_O = 0,4 V$	I_{OLB}	5,0	0,64	0,51	0,36	mA
	$V_O = 0,5 V$	I_{OLB}	10,0	1,60	1,30	0,90	mA
	$V_O = 1,5 V$	I_{OLB}	15,0	4,20	3,40	2,40	mA

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25 °C	T _{amb} HIGH	Unit
Output LOW (sink) current (contd)							
Limited temperature range	V _O = 0,4 V	I _{OLB}	5,0	0,52	0,44	0,36	mA
	V _O = 0,5 V	I _{OLB}	10,0	1,30	1,10	0,90	mA
	V _O = 1,5 V	I _{OLB}	15,0	3,60	3,00	2,40	mA
Output HIGH (source) current							
Full temperature range	V _O = 4,6 V	-I _{OHB}	5,0	0,64	0,51	0,36	mA
	V _O = 9,5 V	-I _{OHB}	10,0	1,60	1,30	0,90	mA
	V _O = 13,5 V	-I _{OHB}	15,0	4,20	3,40	2,40	mA
Limited temperature range	V _O = 4,6 V	-I _{OHB}	5,0	0,52	0,44	0,36	mA
	V _O = 9,5 V	-I _{OHB}	10,0	1,30	1,10	0,90	mA
	V _O = 13,5 V	-I _{OHB}	15,0	3,60	3,00	2,40	mA
Input leakage current	V _{IL} = 0 V V _{IH} = V _{DD}						
Full temperature range		I _{IA}	15,0	0,10	0,10	1,00	µA
Limited temperature range		I _{IA}	15,0	0,30	0,30	1,00	µA
Input capacitance per unit load (Any input)	V _I = 0 V	C _{IA}	-	-	7,5	-	pF
Noise margin at LOW level output (equal to the difference between V _{IL} and V _{OL} for worst case combinations)		V _{NLB} V _{NLB} V _{NLB}	5,0 10,0 15,0	1,0 2,0 2,5	1,0 2,0 2,5	1,0 2,0 2,5	V V V
Noise margin at HIGH level output (equal to the difference between V _{IH} and V _{OH} for worst case combinations)		V _{NHB} V _{NHB} V _{NHB}	5,0 10,0 15,0	1,0 2,0 2,5	1,0 2,0 2,5	1,0 2,0 2,5	V V V

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25 °C	T _{amb} HIGH	Unit
Propagation Delay Time. LOW to HIGH level. BCD input to any segment.		t _{PLHA}	5,0	-	1210,0	-	ns
		t _{PLHA}	10,0	-	500,0	-	ns
		t _{PLHA}	15,0	-	370,0	-	ns
Propagation Delay Time. HIGH to LOW level. BCD input to any segment.		t _{PHLA}	5,0	-	1650,0	-	ns
		t _{PHLA}	10,0	-	660,0	-	ns
		t _{PHLA}	15,0	-	495,0	-	ns
Transition Time LOW to HIGH and HIGH to LOW level		t _{TLHA} /	5,0	-	200,0	-	ns
		t _{THLA}	10,0	-	100,0	-	ns
		t _{TLHA} /					
		t _{THLA}	15,0	-	80,0	-	ns
		t _{TLHA} /					
Set-up Time		t _{su}	5,0	-	0	-	ns
		t _{su}	10,0	-	0	-	ns
		t _{su}	15,0	-	0	-	ns
Hold Time		t _h	5,0	-	80,0	-	ns
		t _h	10,0	-	30,0	-	ns
		t _h	15,0	-	20,0	-	ns
Latch Disable Pulse Width (Strobing Data)		t _{WH}	5,0	-	250,0	-	ns
		t _{WH}	10,0	-	100,0	-	ns
		t _{WH}	15,0	-	80,0	-	ns

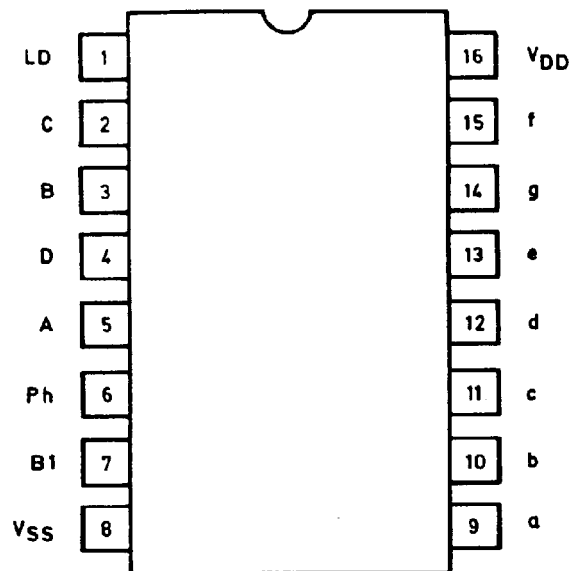


Figure 1

Function Table

Table 1

INPUTS							OUTPUTS							
LD	B1	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
X	H	L	X	X	X	X	L	L	L	L	L	L	L	Blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	Blank
H	L	L	X	X	X	X	**							**
†	†	†	†	†	†	†	Inverse of Output Combinations Above							Display as above

H = High level

L = Low level

X = Level irrelevant

† = Above combinations

* = For liquid crystal readouts, apply a square wave to Ph.

For common cathode LED readouts, select Ph = 0.

For common anode LED readouts, select Ph = 1.

** = Depends upon the BCD code previously applied when LD = 1.

Connections to segments

$$\begin{array}{c} a \\ f \overline{b} / b \\ e \overline{g} / c \\ d \end{array}$$

Display

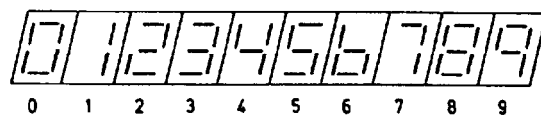


Figure 2

Logic diagram

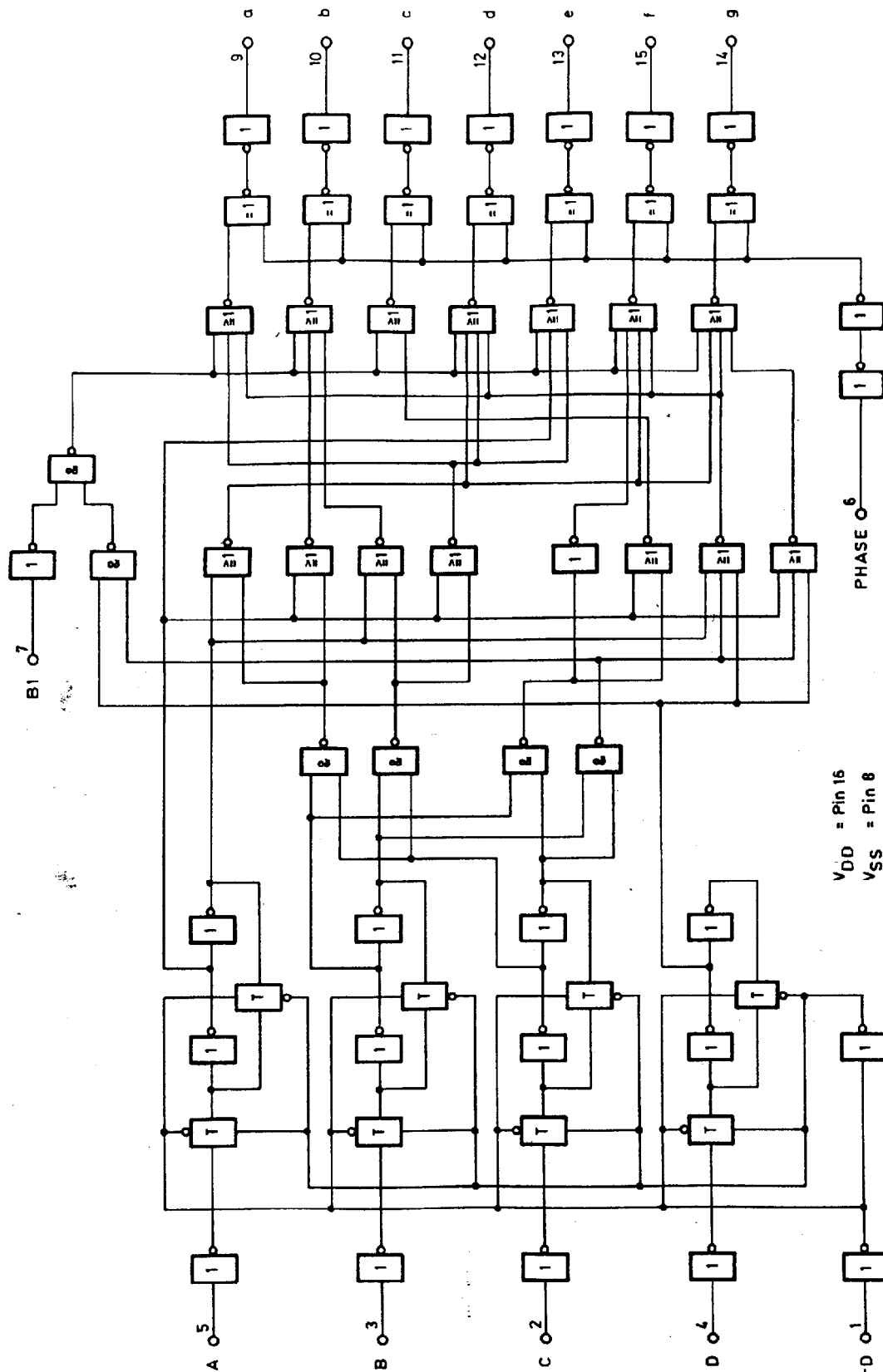


Figure 3