

BRITISH STANDARDS INSTITUTION

2 PARK STREET, LONDON, W1A 2BS

Specification available from:- AS SHOWN IN PD 9002
AND CECC 00 200 AND

MOTOROLA LTD,
KELVIN ESTATE,
EAST KILBRIDE.
G75 0TG

BS CECC 90 104 - 221

ISSUE 1

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Page 1 of 34 pages

ELECTRONIC COMPONENTS OF ASSESSED QUALITY

DETAIL SPECIFICATION IN ACCORDANCE WITH:

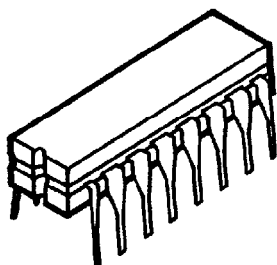
BS CECC 90 000 : 1982
BS CECC 90 100 : 1983

MANUFACTURERS TYPE NUMBER

4551B

SEE PD 9002 AND CECC 00 200
For ordering information
see page 14

Outline not to scale: Isometric projection
Marking information see page 14



QUAD 2-INPUT ANALOGUE
MULTIPLEXER/DEMULTIPLEXER

SILICON COMPLEMENTARY MOS.
WITH (B) BUFFERED OUTPUTS AND
CAVITY PACKAGING.

Assessment levels
R, T and V
and optional screening
categories A, B, C and D

For detail dimensions see IEC 191-2 (A50C)

CAUTION: THESE ARE STATIC SENSITIVE DEVICES - See clause 1.11

1. Limiting conditions of use (not for inspection purposes)

All voltages referenced to V_{SS}

1.1	Maximum supply voltage, positive	V_{DD}	+18,0 V
1.2	Maximum supply voltage, negative	V_{DD}	-0,5 V
1.3	Maximum positive input voltage	V_{IN}	$V_{DD} + 0,5 V$
1.4	Maximum negative input voltage	V_{IN}	-0,5 V

Refer to Qualified Products List PD 9002 and/or CECC 00 200
for details of manufacturers approved to this specification

1.	<u>Limiting conditions of use</u> (cont'd)		
1.5	Maximum power dissipation, per package	P_{D1}	2,9 W
	per output	P_{D2}	360 mW
1.6	Maximum continuous current into any input.	$ I_I $	10,0 mA
1.7	Maximum continuous current into any output.	$ I_O $	10,0 mA
1.8	Operating temperature range	T_{amb}	
		Full	-55 to +125 °C
		Limited	-40 to + 85 °C
1.9	Storage temperature range	T_{stg}	-65 to +150 °C
1.10	Transient energy rating		400 V at 100 pF through 1,5 kΩ
1.11	<u>Recommended handling precautions</u>		
1.11.1	Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method.		
1.11.2	Use grounded tip soldering irons.		
1.11.3	Ground all test equipment.		
1.11.4	Connect all unused device inputs to V_{DD} or V_{SS} .		
1.11.5	PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations.		
1.11.6	Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices.		
1.11.7	Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during inspection or handling.		
1.11.8	When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage, 'Dummy connectors' should be used to electrically short all PC board terminals together.		
1.11.9	Switch off power supply before inserting or removing devices from circuits.		
1.11.10	Disconnect all low impedance equipment and input signals from the device before d.c. power supplies are switched off.		

2. Recommended conditions of use and associated characteristics (not for inspection purposes)

These apply over the operating temperature range unless otherwise stated. All voltages referenced to V_{SS} .

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25 °C	T_{amb} HIGH	Unit
Quiescent device current	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$						
Full temperature range	Outputs open circuit	I_{DDA}	5,0	5,0	5,0	150,0	μA
		I_{DDA}	10,0	10,0	10,0	300,0	μA
		I_{DDA}	15,0	20,0	20,0	600,0	μA
Limited temperature range		I_{DDA}	5,0	20,0	20,0	150,0	μA
		I_{DDA}	10,0	40,0	40,0	300,0	μA
		I_{DDA}	15,0	80,0	80,0	600,0	μA
LOW level output voltage at $ I_O < 1,0 \mu A$	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$	V_{OLA}	5,0	0,05	0,05	0,05	V
		V_{OLA}	10,0	0,05	0,05	0,05	V
		V_{OLA}	15,0	0,05	0,05	0,05	V
HIGH level output voltage at $ I_O < 1,0 \mu A$	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$	V_{OHB}	5,0	4,95	4,95	4,95	V
		V_{OHB}	10,0	9,95	9,95	9,95	V
		V_{OHB}	15,0	14,95	14,95	14,95	V
LOW level output voltage (for worst case combinations) at $ I_O < 1,0 \mu A$	$V_{IL} = 1,5 V$ $V_{IL} = 3,0 V$ $V_{IL} = 4,0 V$	V_{OLA}	5,0	0,5	0,5	0,5	V
		V_{OLA}	10,0	1,0	1,0	1,0	V
		V_{OLA}	15,0	1,5	1,5	1,5	V
HIGH level output voltage (for worst case combinations) at $ I_O < 1,0 \mu A$	$V_{IH} = 3,5 V$ $V_{IH} = 7,0 V$ $V_{IH} = 11,0 V$	V_{OHB}	5,0	4,5	4,5	4,5	V
		V_{OHB}	10,0	9,0	9,0	9,0	V
		V_{OHB}	15,0	13,5	13,5	13,5	V
Input leakage current	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range		$ I_{IA} $	15,0	0,10	0,10	1,00	μA
Limited temperature range		$ I_{IA} $	15,0	0,30	0,30	1,00	μA

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25°C	T _{amb} HIGH	Unit
Input capacitance Control, Inhibit Switch Inputs (Inhibit = 1)	V _I = 0V f = 1MHz	C _{IA}	-	-	7,50	-	pF
		C _{IA}	-	-	21,0	-	pF
Noise margin at LOW level output (equal to the difference between V _{IL} and V _{OL} for worst case combinations)		V _{NLB}	5,0	1,0	1,0	1,0	V
		V _{NLB}	10,0	2,0	2,0	2,0	V
		V _{NLB}	15,0	2,5	2,5	2,5	V
Noise margin at HIGH level output (equal to the difference between V _{IH} and V _{OH} for worst case combinations)		V _{NHB}	5,0	1,0	1,0	1,0	V
		V _{NHB}	10,0	2,0	2,0	2,0	V
		V _{NHB}	15,0	2,5	2,5	2,5	V
Output Capacitance		C _{OUT}	-	17 Typ	-	-	pF
Feedthrough Capacitance		C _{IA-OUT}	-	0,10 Typ	-	-	pF
Total Supply Current		I _T	5,0	I _T = (0,007 µA/kHz) f + I _Q			µA
		I _T	10,0	I _T = (0,20 µA/kHz) f + I _Q			µA
		I _T	15,0	I _T = (0,36 µA/kHz) f + I _Q			µA
On Resistance Full temperature range Limited temperature range		R _{ON}	5,0	800	1050	1300	Ω
		R _{ON}	10,0	400	500	550	Ω
		R _{ON}	15,0	220	280	320	Ω
		R _{ON}	5,0	880	1050	1200	Ω
		R _{ON}	10,0	450	500	520	Ω
		R _{ON}	15,0	250	280	300	Ω
Δ ON resistance between any two channels		ΔR _{ON}	5,0	-	25 Typ	-	Ω
		ΔR _{ON}	10,0	-	10 Typ	-	Ω
		ΔR _{ON}	15,0	-	5,0 Typ	-	Ω

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25°C	T _{amb} HIGH	Unit
OFF channel Leakage current Full temperature range Any channel All channels off			15,0 15,0	±100 ±100	±100 ±100	±1000 ±1000	nA nA
OFF channel Leakage current Limited temperature range Any channel All channels off			15,0 15,0	±300 ±300	±300 ±300	±1000 ±1000	nA nA
Propagation Delay Times LOW to HIGH and HIGH to LOW level Switch input to Switch output	R _L = 10 kΩ	t _{PLHA} / t _{PHLA}	5,0 10,0 15,0	- - -	90,0 40,0 30,0	- - -	ns ns ns
Inhibit to Output Output HIGH or LOW to HIGH Impedance, or HIGH Impedance to HIGH to LOW level	R _L = 10 kΩ	t _{PLZA} / t _{PHZA}	5,0 10,0 15,0	- - -	900,0 375,0 300,0	- - -	ns ns ns
Propagation Delay time LOW to HIGH, and HIGH to LOW level Control Input to Output	R _L = 10 kΩ	t _{PLHA} / t _{PHLA} t _{PLHA} / t _{PHLA} t _{PLHA} / t _{PHLA}	5,0 10,0 15,0	- - -	875 350 250	- - -	ns ns ns
Sine Wave Distortion	R _L = 1 kΩ f = 1 kHz		10,0	-	0,04 Typ	-	%
Bandwidth	R _L = 1 kΩ, V _{IN} = 1/2 (V _{DD} - V _{EE})p-p, 20 log10 $\frac{V_{OUT}}{V_{IN}} = -3$ dB	BW	10,0	-	55 Typ	-	MHz

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Frequency below which switch isolation exceeds 50 dB.	$R_L = 1\text{ k}\Omega$ $V_{IN} = \frac{1}{2}$ $(V_{DD} - V_{EE})_{p-p}$, $20 \log_{10} \frac{V_{OUT}}{V_{IN}} = -50\text{dB}$	-	10,0	-	3,0 Typ	-	MHz
Frequency below which channel separation is better than 50 dB.	$R_L = 1\text{ k}\Omega$ $V_{IN} = \frac{1}{2}$ $(V_{DD} - V_{EE})_{p-p}$, $20 \log_{10} \frac{V_{OUT}(B)}{V_{IN}(A)} = -50\text{dB}$	-	10,0	-	3,0 Typ	-	MHz
Feedthrough Control, Input to Output	$R_1 = 1\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$, Control/Inhibit $t_r = t_f = 20\text{ ns}$	-	10,0	-	30 Typ	-	mV
Maximum Control Frequency	$R_L = 1\text{ k}\Omega$, $V_{OUT} = \frac{1}{2} V_{IN}$		10,0	-	10 Typ	-	MHz

Terminal identification

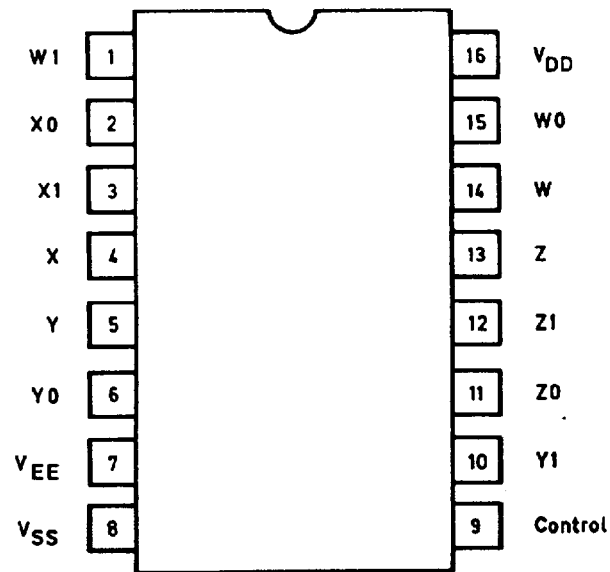


Figure 1

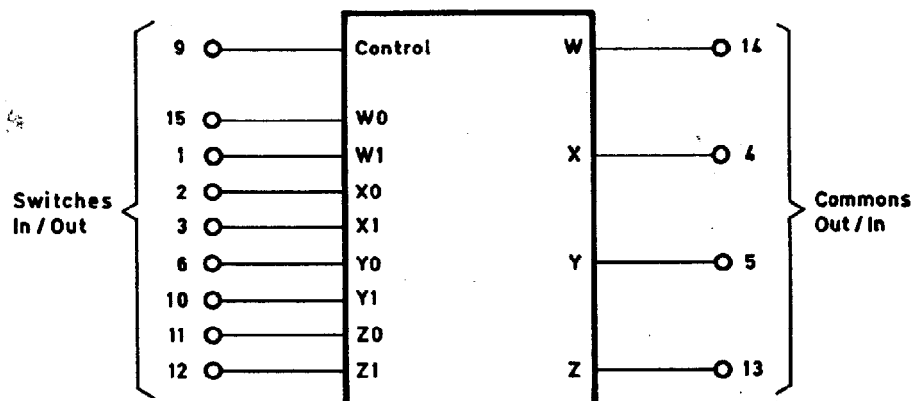


Figure 2

Refer to Table 1

Table 1

Control	ON
L	W0 X0 Y0 Z0
H	W1 X1 Y1 Z1

H = HIGH level

L = LOW level

V_{DD} = Pin 16

V_{SS} = Pin 8

V_{EE} = Pin 7

Note: Control input referenced to V_{SS} , Analogue Inputs and Outputs reference to V_{EE} . V_{EE} must be $\leq V_{SS}$.

Logic diagram

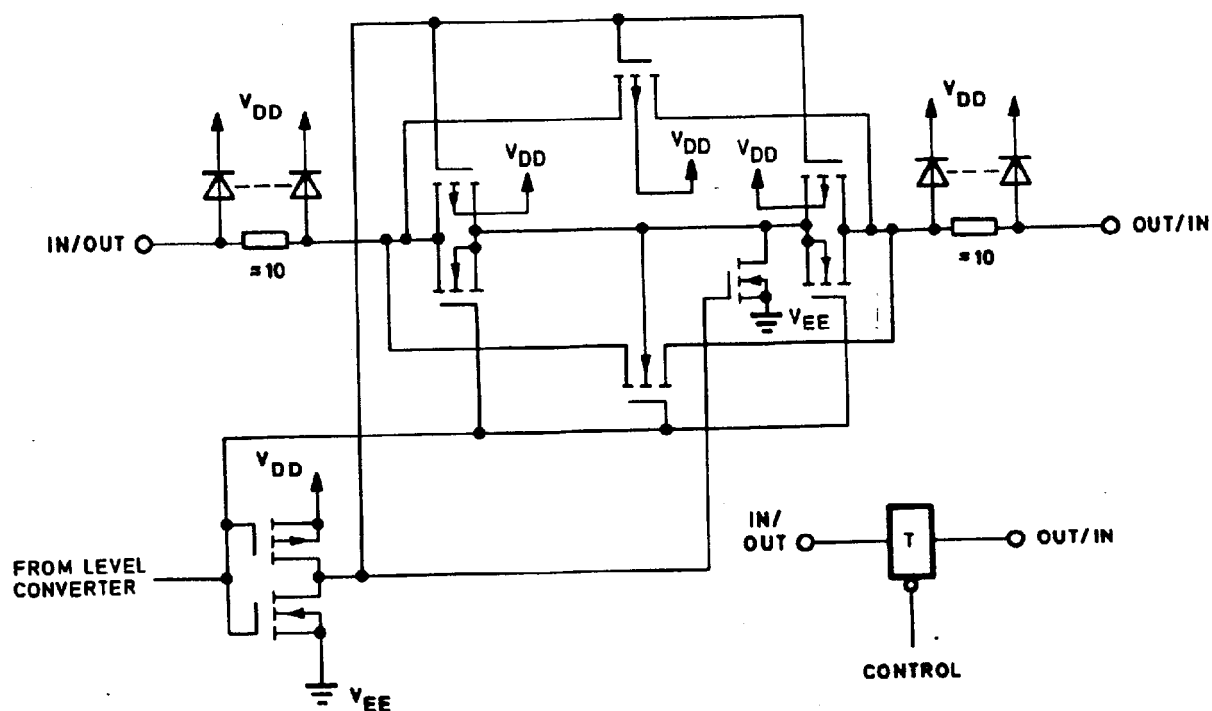


Figure 3

Switch Circuit Schematic

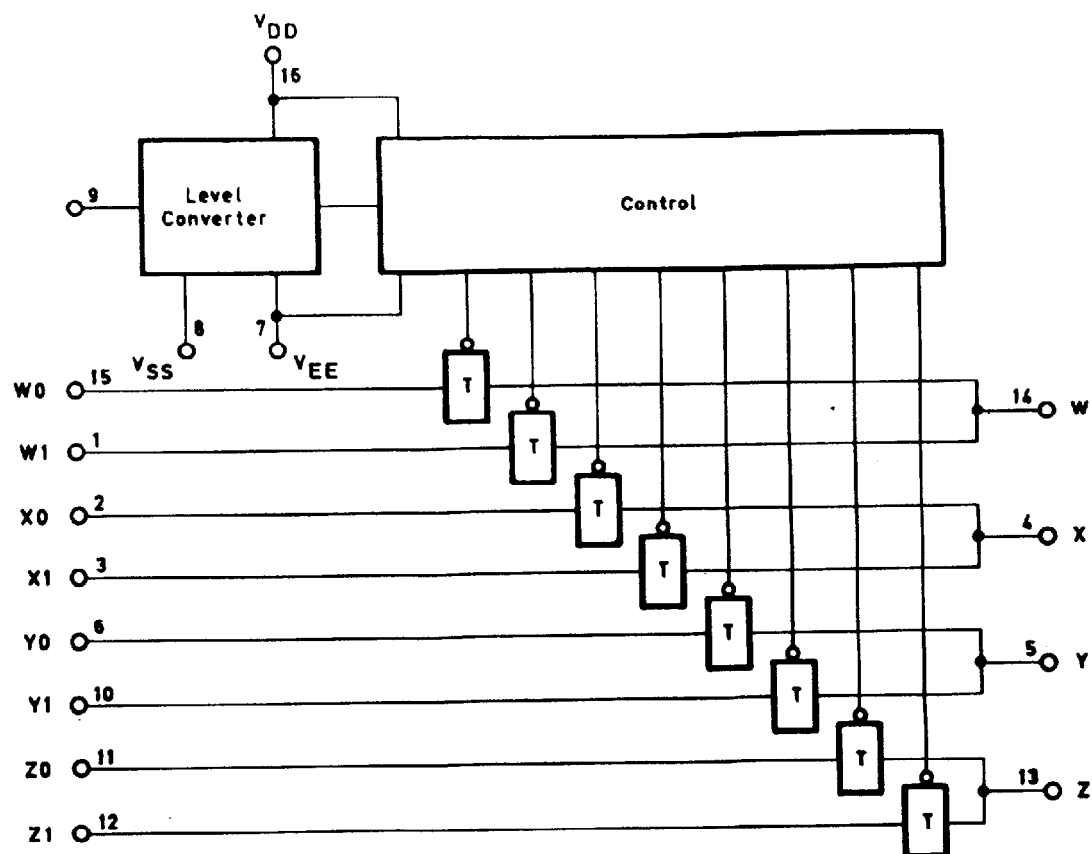


Figure 4

Test Circuits

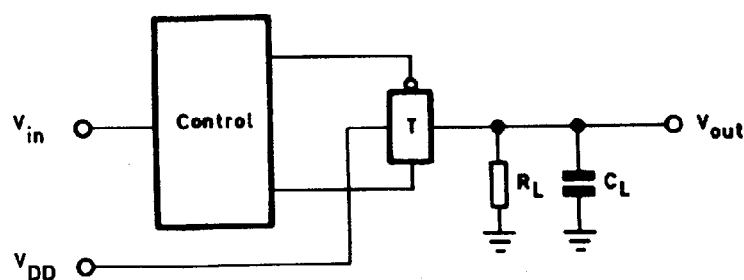


Figure 5 - Input Voltage

Test Circuits (cont'd)

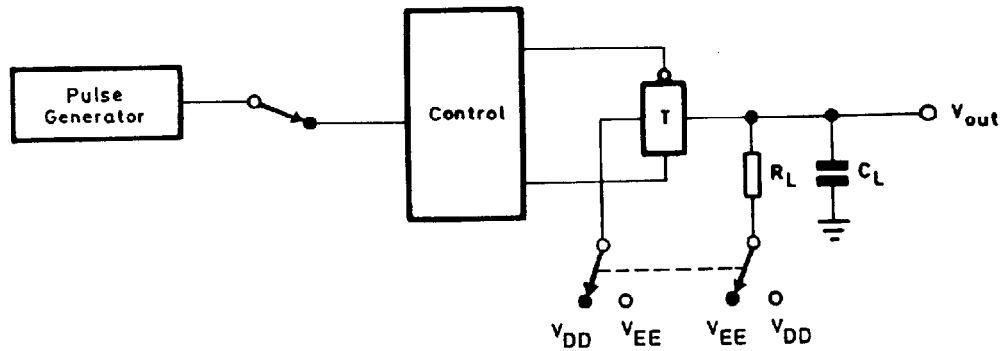


Figure 6 - Propagation Delay times, Control and Inhibit to Output

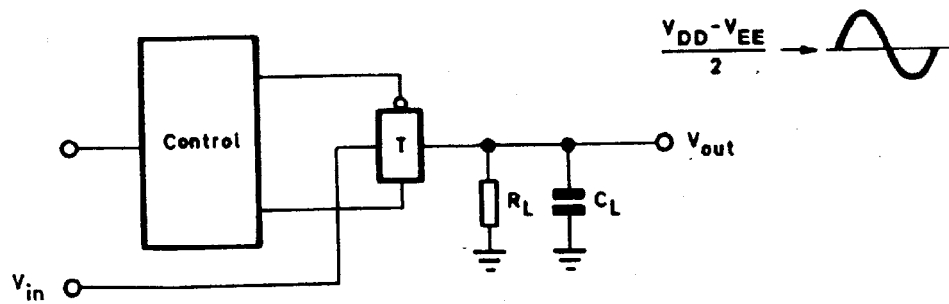


Figure 7 - Bandwidth and Feedthrough Attenuation

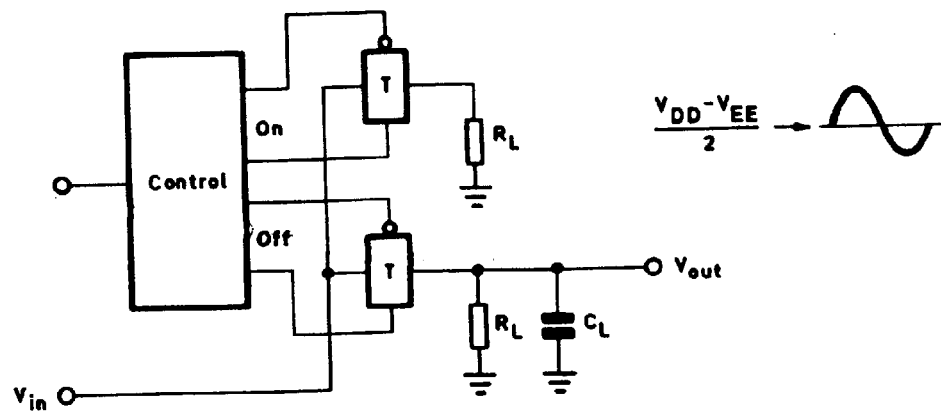


Figure 8 - Crosstalk between any two switches

Test Circuits (cont'd)

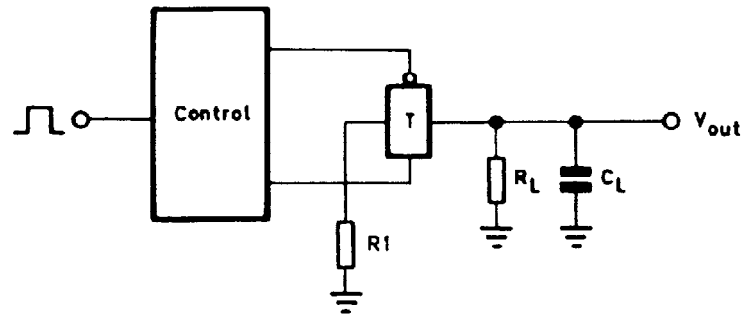
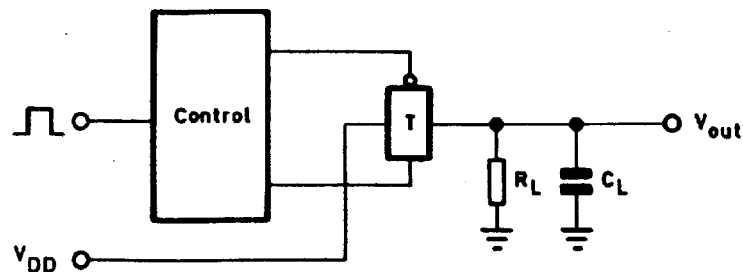


Figure 9 - Feedthrough, Control to Signal Output



$\frac{1}{2}(V_{DD}-V_{EE})$

Figure 10 - Maximum Control Frequency

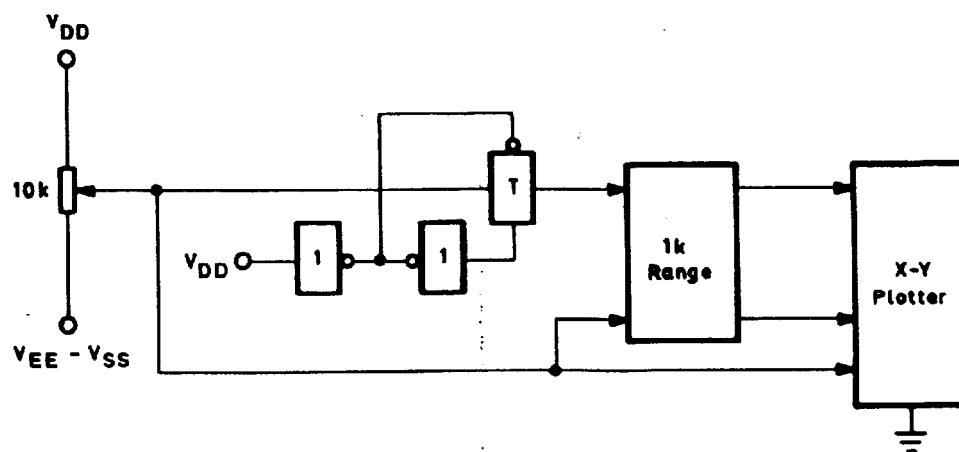


Figure 11 - Channel resistance (R_{ON}) Test Circuit