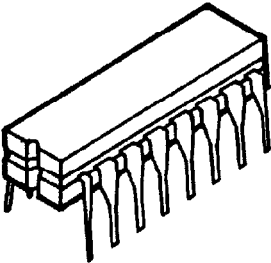


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BRITISH STANDARDS INSTITUTION 2 PARK STREET, LONDON, W1A 2BS Specification available from:- AS SHOWN IN PD 9002 AND CECC 00 200 AND MOTOROLA LTD, KELVIN ESTATE, EAST KILBRIDE. G75 0TG	BS CECC 90 104 - 222 ISSUE 1 AUGUST 1985 Page 1 of 35 pages
ELECTRONIC COMPONENTS OF ASSESSED QUALITY DETAIL SPECIFICATION IN ACCORDANCE WITH: BS CECC 90 000 : 1982 BS CECC 90 100 : 1983	MANUFACTURERS TYPE NUMBER 4553B SEE PD 9002 AND CECC 00 200 For ordering information see page 14
Outline not to scale: Isometric projection Marking information see page 13  For detail dimensions see IEC 191-2 (A50C)	THREE-DIGIT BCD COUNTER SILICON COMPLEMENTARY MOS. WITH (B) BUFFERED OUTPUTS AND CAVITY PACKAGING. Assessment levels R, T and V and optional screening categories A, B, C and D

CAUTION: THESE ARE STATIC SENSITIVE DEVICES - See clause 1.11

1. Limiting conditions of use (not for inspection purposes)

All voltages referenced to V_{SS}

1.1	Maximum supply voltage, positive	V_{DD}	+18,0 V
1.2	Maximum supply voltage, negative	V_{DD}	-0,5 V
1.3	Maximum positive input voltage	V_{IN}	$V_{DD} + 0,5 V$
1.4	Maximum negative input voltage	V_{IN}	-0,5 V

Refer to Qualified Products List PD 9002 and/or CECC 00 200
 for details of manufacturers approved to this specification

1. Limiting conditions of use (contd)

1.5	Maximum power dissipation, per package	P_{D1}	702 mW
	per output	P_{D2}	88 mW
1.6	Maximum continuous current into any input.	I_I	10,0 mA
1.7	Maximum continuous current into any output.	I_O	20,0 mA
1.8	Operating temperature range	T_{amb}	
		Full	-55 to +125 °C
		Limited	-40 to + 85 °C
1.9	Storage temperature range	T_{stg}	-65 to +150 °C
1.10	Transient energy rating		400 V at 100 pF through 1,5 kΩ
1.11	<u>Recommended handling precautions</u>		
1.11.1	Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method.		
1.11.2	Use grounded tip soldering irons.		
1.11.3	Ground all test equipment.		
1.11.4	Connect all unused device inputs to V_{DD} or V_{SS} .		
1.11.5	PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations.		
1.11.6	Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices.		
1.11.7	Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during inspection or handling.		
1.11.8	When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage, 'Dummy connectors' should be used to electrically short all PC board terminals together.		
1.11.9	Switch off power supply before inserting or removing devices from circuits.		
1.11.10	Disconnect all low impedance equipment and input signals from the device before d.c. power supplies are switched off.		

Recommended conditions of use and associated characteristics (not for inspection purposes)

These apply over the operating temperature range unless otherwise stated. All voltages referenced to V_{SS} .

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25 °C	T_{amb} HIGH	Unit
Quiescent device current	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$						
Full temperature range	Outputs open circuit	I_{DDA}	5,0	5,0	5,0	150,0	μA
		I_{DDA}	10,0	10,0	10,0	300,0	μA
		I_{DDA}	15,0	20,0	20,0	600,0	μA
Limited temperature range		I_{DDA}	5,0	50,0	50,0	375,0	μA
		I_{DDA}	10,0	100,0	100,0	750,0	μA
		I_{DDA}	15,0	200,0	200,0	1500,0	μA
LOW level output voltage at $ I_O < 1,0 \mu A$	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$	V_{OLA}	5,0	0,05	0,05	0,05	V
		V_{OLA}	10,0	0,05	0,05	0,05	V
		V_{OLA}	15,0	0,05	0,05	0,05	V
HIGH level output voltage at $ I_O < 1,0 \mu A$	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$	V_{OHB}	5,0	4,95	4,95	4,95	V
		V_{OHB}	10,0	9,95	9,95	9,95	V
		V_{OHB}	15,0	14,95	14,95	14,95	V
LOW level output voltage (for worst case combinations) at $ I_O < 1,0 \mu A$	$V_{IL} = 1,5 V$	V_{OLA}	5,0	0,5	0,5	0,5	V
	$V_{IL} = 3,0 V$	V_{OLA}	10,0	1,0	1,0	1,0	V
	$V_{IL} = 4,0 V$	V_{OLA}	15,0	1,5	1,5	1,5	V
HIGH level output voltage (for worst case combinations) at $ I_O < 1,0 \mu A$	$V_{IH} = 3,5 V$	V_{OHB}	5,0	4,5	4,5	4,5	V
	$V_{IH} = 7,0 V$	V_{OHB}	10,0	9,0	9,0	9,0	V
	$V_{IH} = 11,0 V$	V_{OHB}	15,0	13,5	13,5	13,5	V

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25 °C	T_{amb} HIGH	Unit
Output LOW (sink) current (Pin 3)							
Full temperature range	$V_O = 0,4 V$	I_{OLB}	5,0	0,5	0,4	0,28	mA
	$V_O = 0,5 V$	I_{OLB}	10,0	1,1	0,9	0,65	mA
	$V_O = 1,5 V$	I_{OLB}	15,0	1,8	1,5	1,20	mA
Limited temperature range	$V_O = 0,4 V$	I_{OLB}	5,0	0,23	0,2	0,16	mA
	$V_O = 0,5 V$	I_{OLB}	10,0	0,60	0,5	0,40	mA
	$V_O = 1,5 V$	I_{OLB}	15,0	1,80	1,5	1,20	mA
Output LOW (sink) current (other outputs)							
Full temperature range	$V_O = 0,4 V$	I_{OLB}	5,0	3,0	2,5	1,6	mA
	$V_O = 0,5 V$	I_{OLB}	10,0	6,0	5,0	3,5	mA
	$V_O = 1,5 V$	I_{OLB}	15,0	18,0	15,0	10,0	mA
Limited temperature range	$V_O = 0,4 V$	I_{OLB}	5,0	2,4	2,0	1,6	mA
	$V_O = 0,5 V$	I_{OLB}	10,0	3,8	3,0	2,5	mA
	$V_O = 1,5 V$	I_{OLB}	15,0	10,0	8,4	7,0	mA
Output HIGH (source) current							
Full temperature range	$V_O = 4,6 V$	$-I_{OHB}$	5,0	0,64	0,51	0,36	mA
	$V_O = 9,5 V$	$-I_{OHB}$	10,0	1,60	1,30	0,90	mA
	$V_O = 13,5 V$	$-I_{OHB}$	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_O = 4,6 V$	$-I_{OHB}$	5,0	0,52	0,44	0,36	mA
	$V_O = 9,5 V$	$-I_{OHB}$	10,0	1,30	1,10	0,90	mA
	$V_O = 13,5 V$	$-I_{OHB}$	15,0	3,60	3,00	2,40	mA
Input leakage current	$V_{IL} = 0 V$ $V_{IH} = V_{DD}$						
Full temperature range		$ I_{IA} $	15,0	0,10	0,10	1,00	μA
		$ I_{IA} $	15,0	0,30	0,30	1,00	μA
Limited temperature range							
Input capacitance per unit load (Any input)	$V_I = 0 V$ $f = 1 MHz$	C_{IA}	-	-	7,5	-	pF

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25 °C	T_{amb} HIGH	Unit
Noise margin at LOW level output (equal to the difference between V_{IL} and V_{OL} for worst case combinations)		V_{NLB}	5,0	1,0	1,0	1,0	V
		V_{NLB}	10,0	2,0	2,0	2,0	V
		V_{NLB}	15,0	2,5	2,5	2,5	V
Noise margin at HIGH level output (equal to the difference between V_{IH} and V_{OH} for worst case combinations)		V_{NHB}	5,0	1,0	1,0	1,0	V
		V_{NHB}	10,0	2,0	2,0	2,0	V
		V_{NHB}	15,0	2,5	2,5	2,5	V
Propagation and Transition Times	$C_L = 50$ pF (Test conditions as in Sub-group A5)						
Propagation Delay Time LOW to HIGH and HIGH to LOW level, Clock to BCD Out		$t_{PLHA}/$	5,0	-	1800,0	-	ns
		t_{PHLA}	10,0	-	1000,0	-	ns
			15,0	-	600,0	-	ns
Propagation Delay Time HIGH to LOW level, Clock to Overflow		t_{PHLA}	5,0	-	1200,0	-	ns
			10,0	-	800,0	-	ns
			15,0	-	400,0	-	ns
Propagation Delay Time HIGH to LOW level, Reset to BCD Out		t_{PHLA}	5,0	-	1800,0	-	ns
			10,0	-	1000,0	-	ns
			15,0	-	600,0	-	ns
Transition Time LOW to HIGH and HIGH to LOW level		$t_{TLHA}/$	5,0	-	200,0	-	ns
		t_{THLA}	10,0	-	100,0	-	ns
			15,0	-	80,0	-	ns
Clock to Latch Enable Set-up Time, Latch to Master Reset Set-up Time		t_{set-up}	5,0	-	600,0	-	ns
			10,0	-	400,0	-	ns
			15,0	-	200,0	-	ns

Characteristics	Conditions	Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25 °C	T _{amb} HIGH	Unit
Clock Pulse Width		t _{PWCB}	5,0	-	550,0	-	ns
			10,0	-	200,0	-	ns
			15,0	-	150,0	-	ns
Reset Pulse Width		t _{PWRB}	5,0	-	1200,0	-	ns
			10,0	-	600,0	-	ns
			15,0	-	450,0	-	ns
Input Clock Frequency		F _{cl}	5,0	-	0,9	-	MHz
			10,0	-	2,5	-	MHz
			15,0	-	3,5	-	MHz
Input Clock Rise Time		t _{rA}	5,0	NO LIMIT			
			10,0				
			15,0				
Scan Oscillator Frequency (C1 measured in μF)		F _{osc}	5,0	-	1,5/C TYP		Hz
			10,0	-	4,2/C TYP		Hz
			15,0	-	7,0/C TYP		Hz
Total Supply Current		I _T	5,0	I _T = (0,35 μA/kHz) f + I _{DD}			
			10,0	I _T = (0,85 μA/kHz) f + I _{DD}			
			15,0	I _T = (1,50 μA/kHz) f + I _{DD}			

Terminal identification

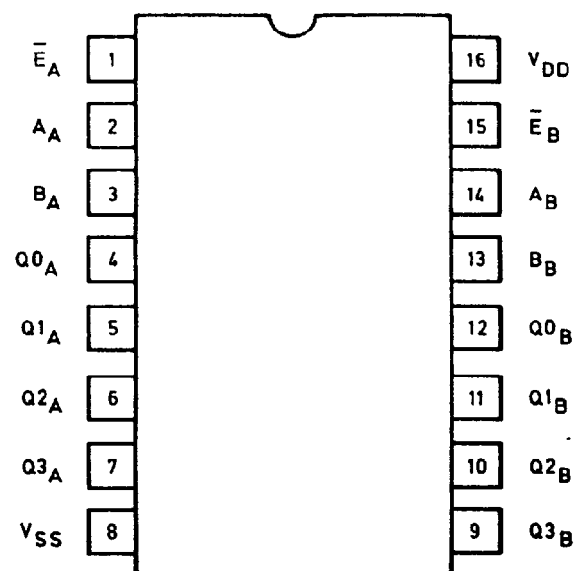


Figure 1

Function Table

Table 1

INPUTS				OUTPUTS
MASTER RESET	CLOCK	DISABLE	LE	
L	↗	L	L	No Change
L	↘	L	L	Advance
L	X	H	X	No Change
L	H	↗	L	Advance
L	H	↘	L	No Change
L	L	X	X	No Change
L	X	X	↗	Latched
L	X	X	H	Latched
H	X	X	L	Q0 = Q1 = Q2 = Q3 = 0

H = High level
 L = Low level
 X = Level irrelevant
 ↗ = Transition low to high level
 ↘ = Transition high to low level

Expanded function block diagram

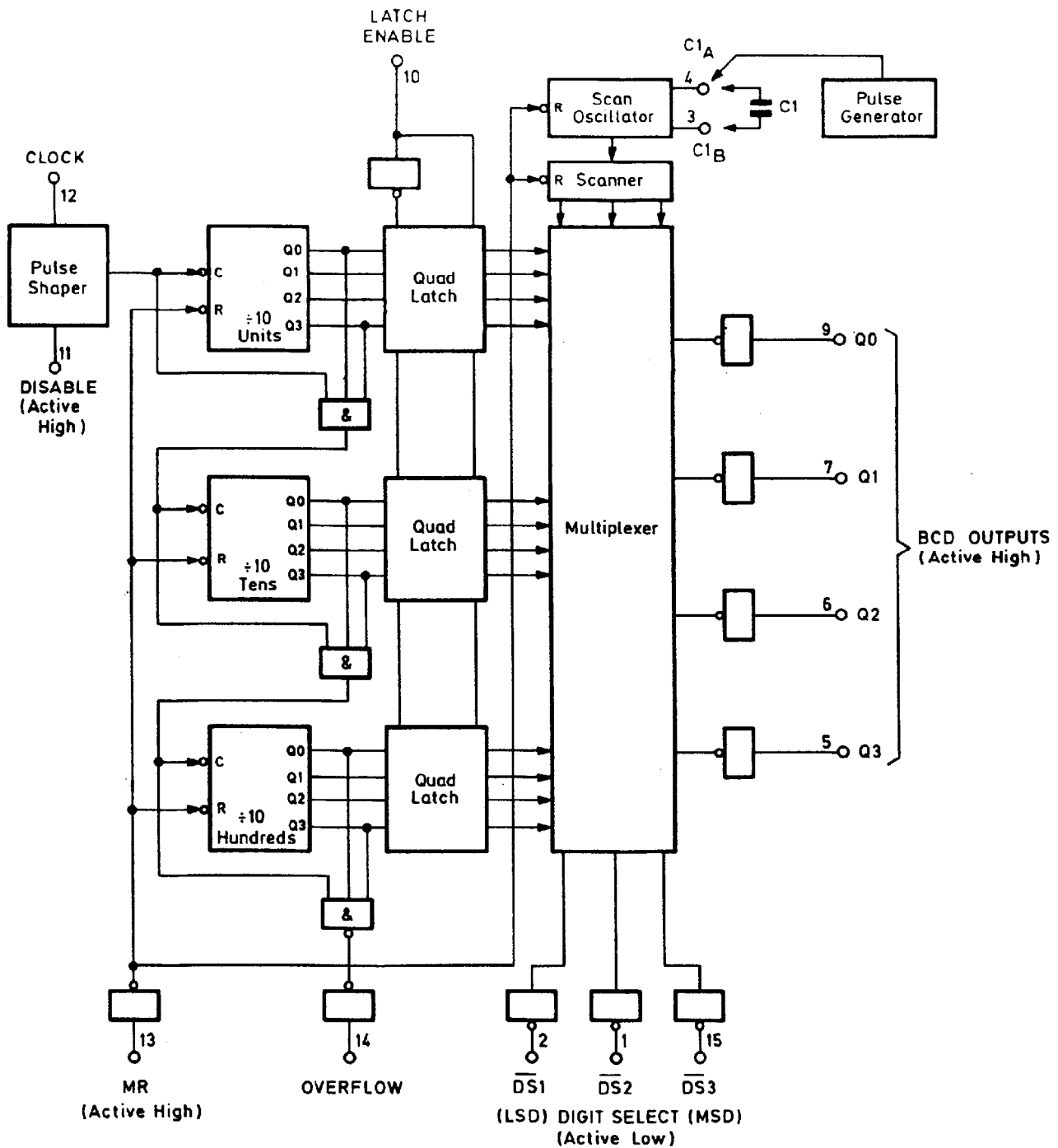


Figure 2

Ambient temperature power derating

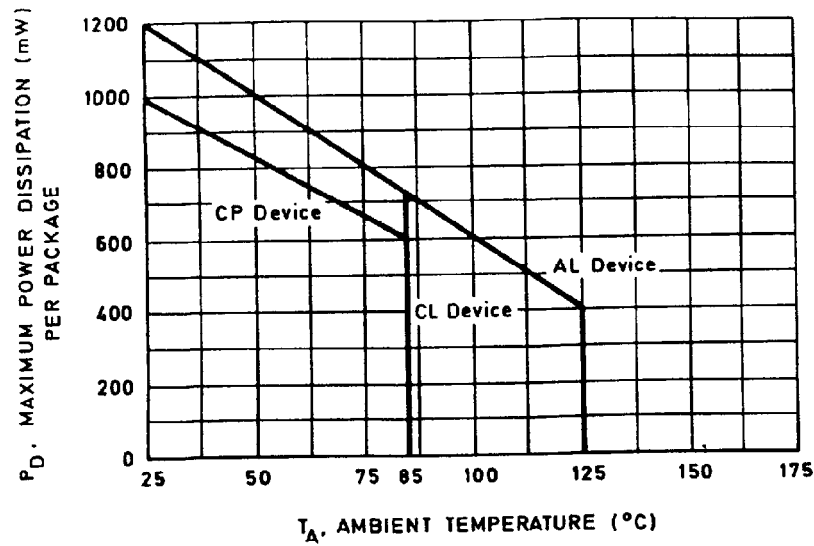


Figure 3