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Specification available from:-

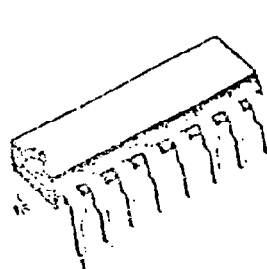
COMITATO ELETTRONICO ITALIANO - Viale Monza 259
20126 MILANO MI (Italy)ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:

CECC 90 000 : 1976

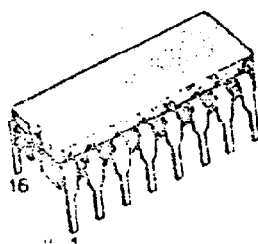
CECC 90 100 : 1977

MANUFACTURERS TYPE NUMBER

4098 B

SEE CECC 00 200
For ordering information
see page 10Outline not to scale: Isometric projection
Marking information see page 9SILICON CMOS 4098 B WITH
BUFFERED OUTPUTS

NON-CAVITY



CAVITY

DUAL, RETRIGGERABLE,
RESETTABLE MONOSTABLE
MULTIVIBRATOR. CAVITY AND
NON-CAVITY PACKAGEAssessment levels
R, S, T and V
and optional screening
categories A, B, C and D

For detail dimensions see IEC 191-2 (A50C)

CAUTION: THESE ARE STATIC SENSITIVE DEVICES - See clause 1.11

Limiting conditions of use (not for inspection purposes)All voltages referenced to V_{SS}

- 1.1 Maximum supply voltage, positive
- 1.2 Maximum supply voltage, negative
- 1.3 Maximum positive input voltage
- 1.4 Maximum negative input voltage

 V_{DD} +18.0V V_{DD} -0.5V V_I V_{DD} +0.5V V_I -0.5V

1. Limiting conditions of use (contd)

1.5	Maximum power dissipation, per package	P_{D1}	200,0mW
	per output	P_{D2}	50,0mW
1.6	Maximum continuous current into any input.	$ I_{I1} $	10,0mA
1.7	Maximum continuous current into any output.	$ I_{O1} $	10,0mA
1.8	Operating temperature range	T_{amb}	
		Full	-55 to +125°C
		Limited	-40 to + 85°C
1.9	Storage temperature range	T_{stg}	-65 to +150°C
1.10	Transient energy rating		400V at 100pF through 1,5kΩ
1.11	<u>Recommended handling precautions</u>		
1.11.1	Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method.		
1.11.2	Use grounded tip soldering irons.		
1.11.3	Ground all test equipment.		
1.11.4	Connect all unused device inputs to V_{DD} or V_{SS} .		
1.11.5	PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations.		
1.11.6	Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices.		
1.11.7	Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during inspection or handling.		
1.11.8	When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage, 'Dummy connectors' should be used to electrically short all PC board terminals together.		
1.11.9	Switch off power supply before inserting or removing devices from circuits.		
1.11.10	Disconnect all low impedance equipment and input signals from the device before d.c. power supplies are switched off.		

These apply over the operating temperature range unless otherwise stated. All voltages referenced to V_{SS} .

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Quiescent device current	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range	Outputs open circuit	I_{DDA}	5,0	1,0	1,0	30,0	μA
		I_{DDA}	10,0	2,0	2,0	60,0	μA
		I_{DDA}	15,0	4,0	4,0	120,0	μA
Limited temperature range		I_{DDA}	5,0	4,0	4,0	30,0	μA
		I_{DDA}	10,0	8,0	8,0	60,0	μA
		I_{DDA}	15,0	16,0	16,0	120,0	μA
LOW level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OLA}	5,0	0,05	0,05	0,05	V
		V_{OLA}	10,0	0,05	0,05	0,05	V
		V_{OLA}	15,0	0,05	0,05	0,05	V
HIGH level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OHB}	5,0	4,95	4,95	4,95	V
		V_{OHB}	10,0	9,95	9,95	9,95	V
		V_{OHB}	15,0	14,95	14,95	14,95	V
LOW level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IL} = 1,5V$	V_{OLA}	5,0	0,5	0,5	0,5	V
	$V_{IL} = 3,0V$	V_{OLA}	10,0	1,0	1,0	1,0	V
	$V_{IL} = 4,0V$	V_{OLA}	15,0	1,5	1,5	1,5	V
HIGH level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IH} = 3,5V$	V_{OHB}	5,0	4,5	4,5	4,5	V
	$V_{IH} = 7,0V$	V_{OHB}	10,0	9,0	9,0	9,0	V
	$V_{IH} = 11,0V$	V_{OHB}	15,0	13,5	13,5	13,5	V
Output LOW (sink) current							
Full temperature range	$V_O = 0,4V$	I_{OLB}	5,0	0,64	0,51	0,36	mA
	$V_O = 0,5V$	I_{OLB}	10,0	1,60	1,30	0,90	mA
	$V_O = 1,5V$	I_{OLB}	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_O = 0,4V$	I_{OLB}	5,0	0,52	0,44	0,36	mA
	$V_O = 0,5V$	I_{OLB}	10,0	1,30	1,10	0,90	mA
	$V_O = 1,5V$	I_{OLB}	15,0	3,60	3,00	2,40	mA

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Output HIGH (source) current							
Full temperature range	$V_O = 4,6V$	$-I_{OHB}$	5,0	0,64	0,51	0,36	mA
	$V_O = 9,5V$	$-I_{OHB}$	10,0	1,60	1,30	0,90	mA
	$V_O = 13,5V$	$-I_{OHB}$	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_O = 4,6V$	$-I_{OHB}$	5,0	0,52	0,44	0,36	mA
	$V_O = 9,5V$	$-I_{OHB}$	10,0	1,30	1,10	0,90	mA
	$V_O = 13,5V$	$-I_{OHB}$	15,0	3,60	3,00	2,40	mA
Input leakage current	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range		$ I_{IA} $	15,0	0,10	0,10	1,00	μA
Limited temperature range		$ I_{IA} $	15,0	0,30	0,30	1,00	μA
Input capacitance per unit load (Any input)	$V_I = 0V$ $f = 1MHz$	C_{IA}	-	-	7,5	-	pF
Noise margin at LOW level output (equal to the difference between V_{IL} and V_{OL} for worst case combinations)		V_{NLB}	5,0	1,0	1,0	1,0	V
		V_{NLB}	10,0	2,0	2,0	2,0	V
		V_{NLB}	15,0	2,5	2,5	2,5	V
Noise margin at HIGH level output (equal to the difference between V_{IH} and V_{OH} for worst case combinations)		V_{NHB}	5,0	1,0	1,0	1,0	V
		V_{NHB}	10,0	2,0	2,0	2,0	V
		V_{NHB}	15,0	2,5	2,5	2,5	V
Propagation and Transition Times	$C_L = 50pF$ (Test conditions as in Sub-group A5)						

Characteristics	Conditions		Symbol	V _{DD} (V)	T _{amb} LOW	T _{amb} = 25°C	T _{amb} HIGH	Unit
	R _x (kΩ)	C _x (pF)						
Transition Time LOW to HIGH level	5 to 10.000	≥ 15	t _{TLHA}	5,0	-	200,0	-	ns
			t _{TLHA}	10,0	-	100,0	-	ns
			t _{TLHA}	15,0	-	80,0	-	ns
Transition Time HIGH to LOW level	5 to 10.000	15 to 10.000	t _{THLA}	5,0	-	200,0	-	ns
			t _{THLA}	10,0	-	100,0	-	ns
			t _{THLA}	15,0	-	80,0	-	ns
Propagation Delay Time HIGH to LOW and LOW to HIGH level A or B to Q or Q̄	5 to 10.000	≥ 15	t _{PLHA} /	5,0	-	500,0	-	ns
			t _{PHLA}	10,0	-	250,0	-	ns
			t _{PHLA}	15,0	-	200,0	-	ns
Propagation Delay Time HIGH to LOW and LOW to HIGH level C _D to Q or Q̄	5 to 10.000	≥ 15	t _{PLHA} /	5,0	-	450,0	-	ns
			t _{PHLA}	10,0	-	250,0	-	ns
			t _{PHLA}	15,0	-	150,0	-	ns
HIGH or LOW Pulse Width (P _{SET})	100	15	t _{PWHC}	5,0	-	200,0*	-	ns
			t _{PWHC}	10,0	-	80,0	-	ns
			t _{PWHC}	15,0	-	60,0	-	ns
	100	1000	t _{PWHC}	5,0	-	1200,0*	-	ns
			t _{PWHC}	10,0	-	600,0	-	ns
			t _{PWHC}	15,0	-	500,0	-	ns
	100	100.000	t _{PWHC}	5,0	-	50,0*	-	μs
			t _{PWHC}	10,0	-	30,0	-	μs
			t _{PWHC}	15,0	-	20,0	-	μs
Retrigger Time			t _{rrB}	5,0	-	0,0	-	ns
			t _{rrB}	10,0	-	0,0	-	ns
			t _{rrB}	15,0	-	0,0	-	ns
External Timing Resistance			R _{X0}		-	5,0	-	kΩ
			R _{Xn}		-	(1)	-	kΩ

* MINIMUM VALUES

(1) The maximum usable resistance R_X is a function of the leakage of capacitance C_X, the leakage of the device, and the leakage due to board layout and surface resistance

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Documents

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Terminal identification

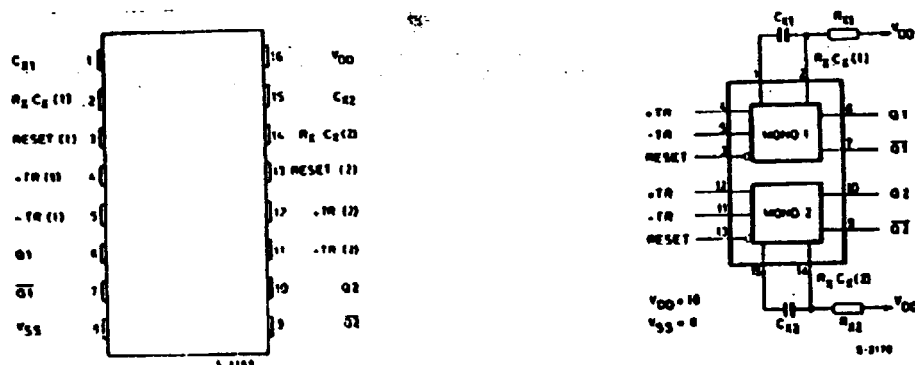
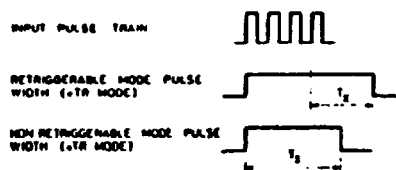


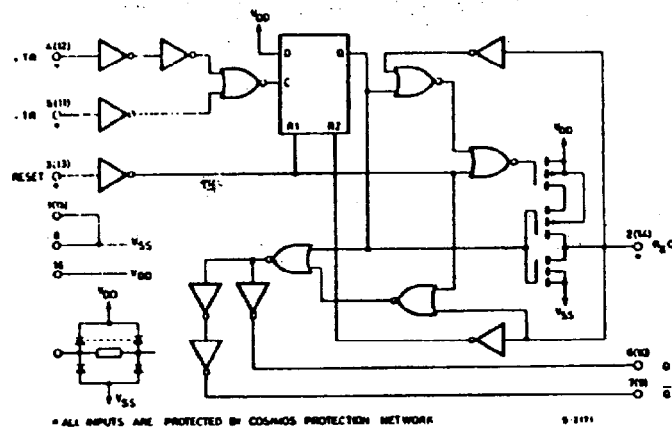
Figure 1

FUNCTION	TERMINAL CONNECTIONS						OTHER CONNECTIONS	
	TO V _{DD}		TO V _{SS}		INPUT PULSE TO			
	Mono(1)	Mono(2)	Mono(1)	Mono(2)	Mono(1)	Mono(2)	Mono(1)	Mono(2)
Leading - Edge Trigger/Retriggerable	3, 5	11, 13			4	12		
Leading - Edge Trigger/Non-retriggerable	3	13			4	12	5, 7	11, 9
Trailing - Edge Trigger/Retriggerable	3	13	4	12	5	11		
Trailing - Edge Trigger/Non-retriggerable	3	13			5	11	4, 6	12, 10
Unused Section	5	11	3, 4	12, 13				

NOTES: 1) A Retriggerable one-shot multivibrator has an output pulse width which is extended one full time period (T_X) after application of the last trigger pulse.
 2) A Non-retriggerable one-shot multivibrator has a time period T_X referenced from the application of the first trigger pulse.



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This is a graphic representation, not a circuit diagram

Figure 2

Switching time waveforms

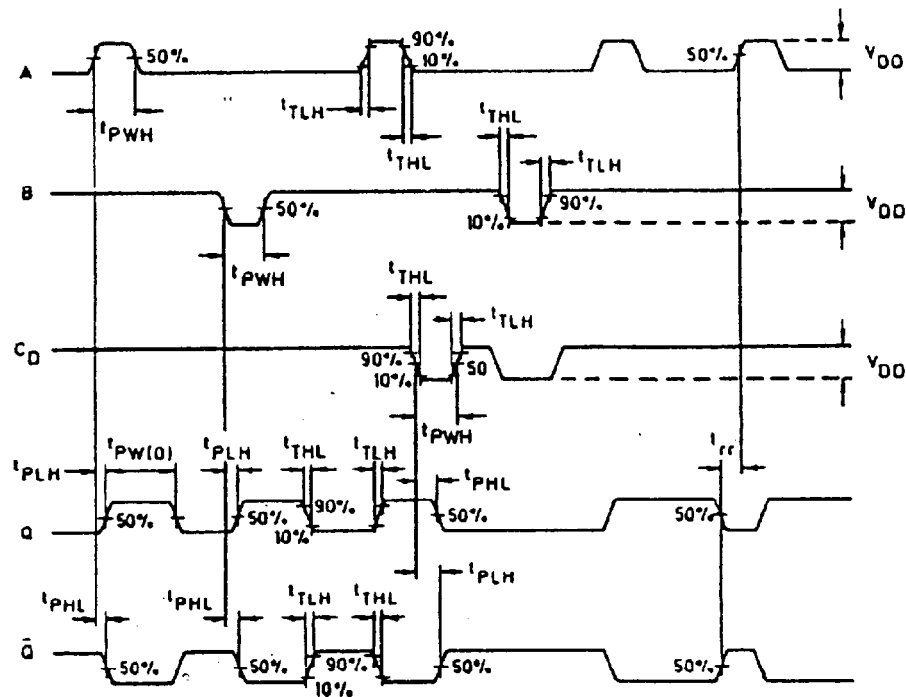


Figure 3