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COMITATO ELETTROTECNICO ITALIANO - Viale Monza 259
20126 MILANO MI (Italy)

ISSUE 1 - 1987

July



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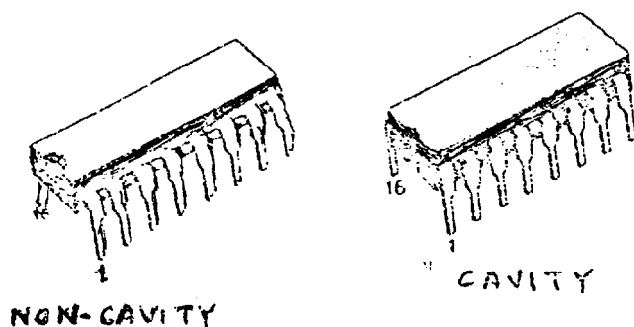
ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:

CECC 90 000 : 1985

CECC 90 100 : 1986

MANUFACTURERS TYPE NUMBER

4047B

SEE GPL - CECC 00 200
For ordering information
see page 10Outline not to scale: Isometric projection
Marking information see page 9SILICON CMOS 4047 B WITH
BUFFERED OUTPUTSLOW POWER
MONOSTABLE/ASTABLE
MULTIVIBRATOR CAVITY AND
NON-CAVITY PACKAGE

For detail dimensions see IEC 191-2 (A50C)

Assessment levels
R, S, T and V
and optional screening
categories A, B, C and D

CAUTION: THESE ARE STATIC SENSITIVE DEVICES - See clause 1.11

1. Limiting conditions of use (not for inspection purposes)All voltages referenced to V_{SS}

- 1.1 Maximum supply voltage, positive
- 1.2 Maximum supply voltage, negative
- 1.3 Maximum positive input voltage
- 1.4 Maximum negative input voltage

 V_{DD} +18,0V V_{DD} -0,5V V_I V_{DD} +0,5V V_I -0,5V

1. Limiting conditions of use (contd)
- 1.5 Maximum power dissipation, per package
per output P_{D1} 200,0mW
 P_{D2} 50,0mW
- 1.6 Maximum continuous current into any input. $|I_I|$ 10,0mA
- 1.7 Maximum continuous current into any output. $|I_O|$ 10,0mA
- 1.8 Operating temperature range T_{amb}
Full -55 to +125°C
Limited -40 to +85°C
- 1.9 Storage temperature range T_{stg} -65 to +150°C
- 1.10 Transient energy rating 400V at 100pF through 1,5kΩ
- 1.11 Recommended handling precautions
- 1.11.1 Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method.
- 1.11.2 Use grounded tip soldering irons.
- 1.11.3 Ground all test equipment.
- 1.11.4 Connect all unused device inputs to V_{DD} or V_{SS} .
- 1.11.5 PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations.
- 1.11.6 Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices.
- 1.11.7 Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during inspection or handling.
- 1.11.8 When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage, 'Dummy connectors' should be used to electrically short all PC board terminals together.
- 1.11.9 Switch off power supply before inserting or removing devices from circuits.
- 1.11.10 Disconnect all low impedance equipment and input signals from the device before d.c. power supplies are switched off.

2. Recommended conditions of use and associated characteristics (not for inspection purposes)

These apply over the operating temperature range unless otherwise stated. All voltages referenced to V_{SS} .

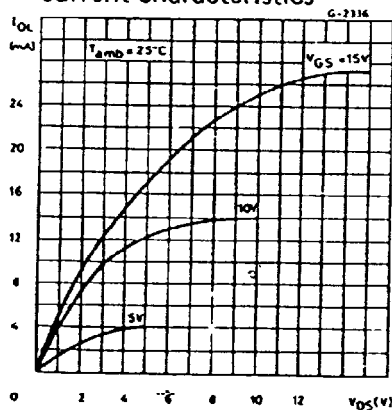
Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Quiescent device current	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range	Outputs open circuit	I_{DDA}	5,0	1,0	1,0	30,0	μA
		I_{DDA}	10,0	2,0	2,0	60,0	μA
		I_{DDA}	15,0	4,0	4,0	120,0	μA
Limited temperature range		I_{DDA}	5,0	4,0	4,0	30,0	μA
		I_{DDA}	10,0	8,0	8,0	60,0	μA
		I_{DDA}	15,0	16,0	16,0	120,0	μA
LOW level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OLA}	5,0	0,05	0,05	0,05	V
		V_{OLA}	10,0	0,05	0,05	0,05	V
		V_{OLA}	15,0	0,05	0,05	0,05	V
HIGH level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OHB}	5,0	4,95	4,95	4,95	V
		V_{OHB}	10,0	9,95	9,95	9,95	V
		V_{OHB}	15,0	14,95	14,95	14,95	V
LOW level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IL} = 1,5V$ $V_{IL} = 3,0V$ $V_{IL} = 4,0V$	V_{OLA}	5,0	0,5	0,5	0,5	V
		V_{OLA}	10,0	1,0	1,0	1,0	V
		V_{OLA}	15,0	1,5	1,5	1,5	V
HIGH level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IH} = 3,5V$ $V_{IH} = 7,0V$ $V_{IH} = 11,0V$	V_{OHB}	5,0	4,5	4,5	4,5	V
		V_{OHB}	10,0	9,0	9,0	9,0	V
		V_{OHB}	15,0	13,5	13,5	13,5	V
Output LOW (sink) current							
Full temperature range	$V_O = 0,4V$	I_{OLB}	5,0	0,64	0,51	0,36	μA
	$V_O = 0,5V$	I_{OLB}	10,0	1,60	1,30	0,90	μA
	$V_O = 1,5V$	I_{OLB}	15,0	4,20	3,40	2,40	μA
Limited temperature range	$V_O = 0,4V$	I_{OLB}	5,0	0,52	0,44	0,36	μA
	$V_O = 0,5V$	I_{OLB}	10,0	1,30	1,10	0,90	μA
	$V_O = 1,5V$	I_{OLB}	15,0	3,60	3,00	2,40	μA

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Output HIGH (source) current							
Full temperature range	$V_O = 4,6V$	$-I_{OHB}$	5,0	0,64	0,51	0,36	mA
	$V_O = 9,5V$	$-I_{OHB}$	10,0	1,60	1,30	0,90	mA
	$V_O = 13,5V$	$-I_{OHB}$	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_O = 4,6V$	$-I_{OHB}$	5,0	0,52	0,44	0,36	mA
	$V_O = 9,5V$	$-I_{OHB}$	10,0	1,30	1,10	0,90	mA
	$V_O = 13,5V$	$-I_{OHB}$	15,0	3,60	3,00	2,40	mA
Input leakage current	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range		$ I_{IA} $	15,0	0,10	0,10	1,00	μA
Limited temperature range		$ I_{IA} $	15,0	0,30	0,30	1,00	μA
Input capacitance per unit load (Any input)	$V_I = 0V$ $f = 1MHz$	C_{IA}	-	-	7,5	-	pF
Noise margin at LOW level output (equal to the difference between V_{IL} and V_{OL} for worst case combinations)		V_{NLB}	5,0	1,0	1,0	1,0	V
		V_{NLB}	10,0	2,0	2,0	2,0	V
		V_{NLB}	15,0	2,5	2,5	2,5	V
Noise margin at HIGH level output (equal to the difference between V_{IH} and V_{OH} for worst case combinations)		V_{NHB}	5,0	1,0	1,0	1,0	V
		V_{NHB}	10,0	2,0	2,0	2,0	V
		V_{NHB}	15,0	2,5	2,5	2,5	V
Propagation and Transition Times	$C_L = 50pF$ (Test conditions as in Sub-group A5)						

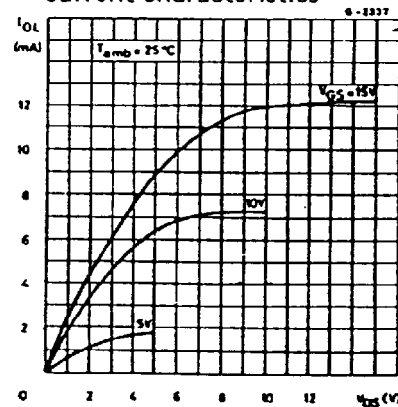
DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $C_L = 15 \text{ pF}$, $R_L = 200 \text{ K}\Omega$, typical temperature coefficient for all V_{DD} values is $0.3\%/^{\circ}\text{C}$, all input rise and fall times = 20 ns)

Parameter			Test conditions	Values			Unit
				$V_{DD} \text{ (V)}$	Min.	Typ.	Max.
t_{PLH} , t_{PHL} Propagation delay time	Astable, Astable to osc. out.			5		200	
				10		100	
				15		70	
		Astable, Astable to Q, $\bar{Q}$		5		550	
				10		250	
				15		150	
	+Trigger, -Trigger to Q, $\bar{Q}$			5		700	
				10		300	
				15		200	
	+Trigger, Retrigger to Q, $\bar{Q}$			5		300	
				10		175	
				15		125	
t_{THL} , t_{TLH} Transition time osc. out Q, $\bar{Q}$				5		100	
				10		50	
				15		40	
							ns
t_W Input pulse width (any input)				5		500	
				10		200	
				15		140	
t_r , t_f +Trigger, Retrigger rise and fall time				5		15	
				10		5	
				15		5	

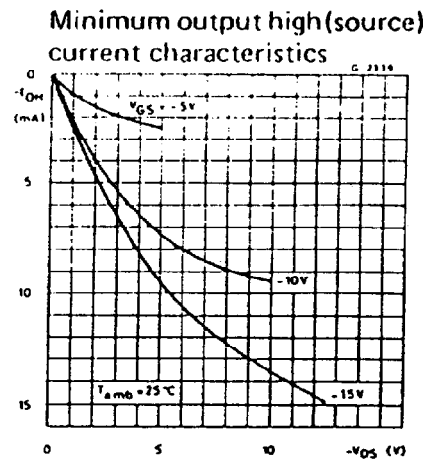
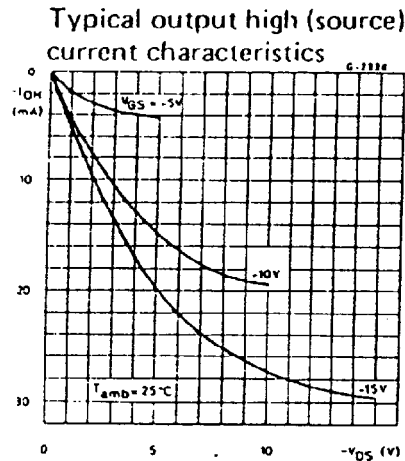
Typical output low (sink) current characteristics



Minimum output low (sink) current characteristics

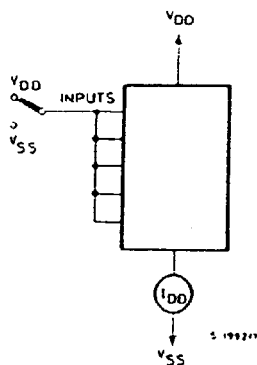


(4) The maximum usable resistance R_X is a function of the leakage of capacitance C_X , the leakage of the device, and the leakage due to board layout and surface resistance

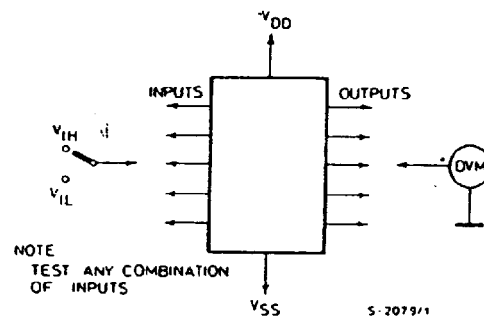


TEST CIRCUITS

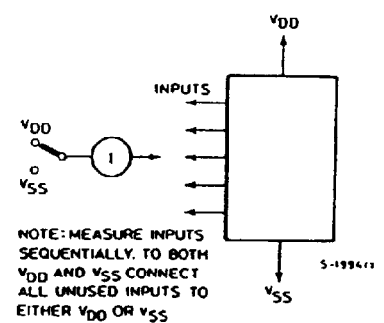
Quiescent device current



Input voltage



Input current



APPLICATION INFORMATION

1 - Circuit description

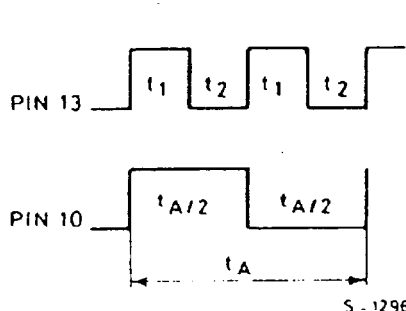
Astable operation is enabled by a high level on the ASTABLE input. The period of the square wave at the Q and $\bar{Q}$ Outputs in this mode of operation is a function of the external components employed. "True" input pulses on the ASTABLE input or "Complement" pulses on the $\overline{\text{ASTABLE}}$ input allow the circuit to be used as a gatable multivibrator. The OSCILLATOR output period will be half of the Q terminal output in the astable mode. However, a 50% duty cycle is not guaranteed at this output. In the monostable mode, positive-edge triggering is accomplished by application of a leading-edge pulse to the +TRIGGER input and a low level to the -TRIGGER input. For negative-edge triggering, a trailing-edge pulse is applied to the -TRIGGER and a high level is applied to the +TRIGGER. Input pulses may be of any duration relative to the output pulse. The multivibrator can be retriggered (on the leading edge only) by applying a common pulse to both the RETRIGGER and +TRIGGER inputs. In this mode the output pulse remains high as long as the input pulse period is shorter than the period determined by the RC components. An external countdown option can be implemented by coupling "Q" to an external "N" counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the $\overline{\text{ASTABLE}}$ input and has a duration equal to N times the period of the multivibrator. A high level on the EXTERNAL RESET input assures no output pulse during an "ON" power condition. This input can also be activated to terminate the output pulse at any time. In the monostable mode, a high-level or power-on reset pulse, must be applied to the EXTERNAL RESET whenever V_{DD} is applied.

APPLICATION INFORMATION (continued)

2 - Astable Mode

The following analysis presents worst-case variations from unit-to-unit as a function of transfer-voltage (V_{TR}) shift (33% - 67% V_{DD}) for free-running (astable) operation.

Astable mode waveforms



$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_{TR}}$$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2 V_{DD} - V_{TR}}$$

$$t_A = 2(t_1 + t_2) = -2 RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2 V_{DD} - V_{TR})}$$

Typ: $V_{TR} = 0.5 V_{DD}$ $t_A = 4.40 RC$

Min: $V_{TR} = 0.33 V_{DD}$ $t_A = 4.62 RC$

Max: $V_{TR} = 0.67 V_{DD}$ $t_A = 4.62 RC$

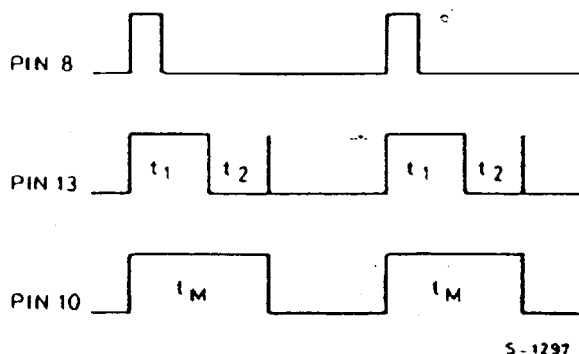
thus if $t_A = 4.40 RC$ is used, the maximum variation will be (+5.0%, -0.0%)

In addition to variations from unit-to-unit, the astable period may vary as a function of frequency with respect to V_{DD} and temperature.

3 - Monostable Mode

The following analysis presents worst-case variations from unit-to-unit as a function of transfer-voltage (V_{TR}) shift (33% - 67% V_{DD}) for one-shot (monostable) operation.

Monostable waveforms



$$t_1 = -RC \ln \frac{V_{TR}}{2 V_{DD}}$$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2 V_{DD} - V_{TR}}$$

$$t_M = (t_1 + t_2) = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(2 V_{DD} - V_{TR})(2 V_{DD})}$$

- 2 -

APPLICATION INFORMATION (continued)

where t_M = monostable mode pulse width. Values for t_M are as follows:

Typ : $V_{TR} = 0.5 V_{DD}$	$t_M = 2.48 RC$
Min : $V_{TR} = 0.33 V_{DD}$	$t_M = 2.71 RC$
Max : $V_{TR} = 0.67 V_{DD}$	$t_M = 2.48 RC$

Thus if $t_M = 2.48 RC$ is used, the maximum variation will be (+9.3%, -0.0%).

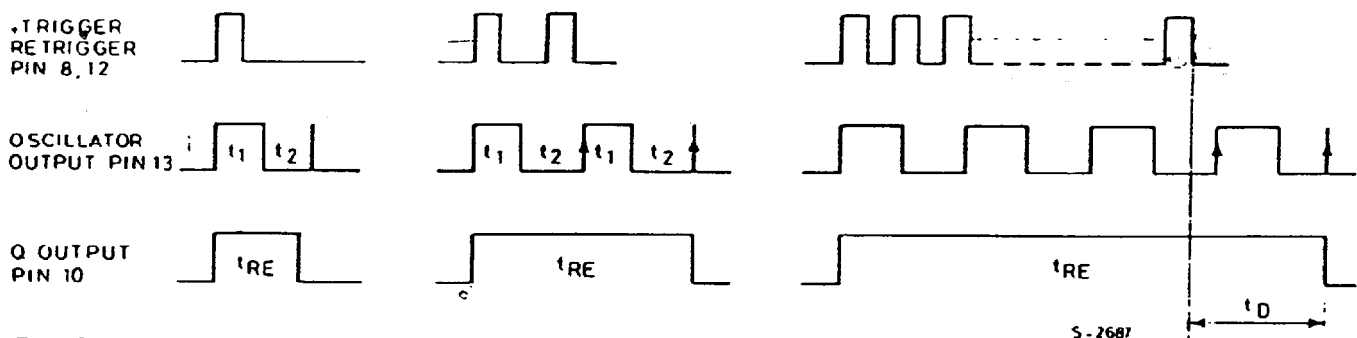
Note: In the astable mode, the first positive half cycle has a duration of T_M ; succeeding durations are $t_A/2$.

In addition to variations from unit to unit, the monostable pulse width may vary as a function of frequency with respect to V_{DD} and temperature.

4 - Retrigger Mode

The HCC/HCF 4047B can be used in the retrigger mode to extend the output-pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to terminals 8 and 12, and the output is taken from terminal 10 or 11. As shown in Fig. A a normal monostable action is obtained when one retrigger pulse is applied. Extended pulse duration is obtained when more than one pulse is applied. For two input pulses, $t_{RE} = t_1' + t_1 + 2t_2$. For more than two pulses, t_{RE} (Q OUTPUT) terminates at some variable time t_D after the termination of the last retrigger pulse. t_D is variable because t_{RE} (Q OUTPUT) terminates after the second positive edge of the oscillator output appears at flip-flop 4 (see logic diagram).

Fig. A - Retrigger-mode waveforms



5 - External Counter Option

Time t_M can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time.

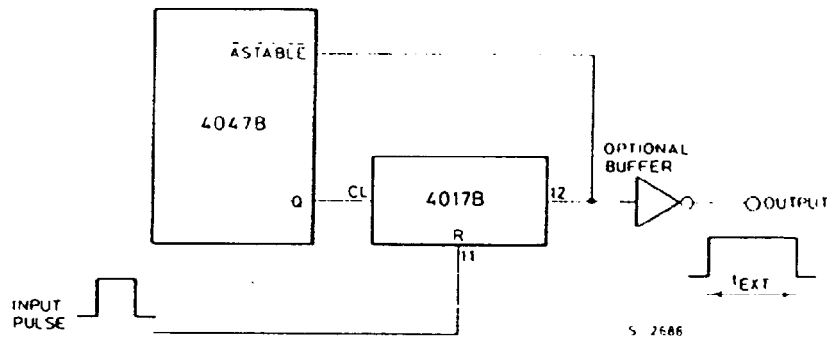
A typical implementation is shown in Fig. B. The pulse duration at the output is

$$t_{ext} = (N - 1) (t_A) + (t_M + t_A/2)$$

where t_{ext} = pulse duration of the circuitry, and N is the number of counts used.

APPLICATION INFORMATION (continued)

Fig. B - Implementation of external counter option



6 - Power Consumption

In the standby mode (Monostable or Astable), power dissipation will be a function of leakage current in the circuit, as shown in the static electrical characteristics. For dynamic operation, the power needed to charge the external timing capacitor C is given by the following formula:

Astable Mode: $P = 2CV^2f$. (Output at Pin 13)
 $P = 4CV^2f$. (Output at Pin 10 and 11)

Monostable Mode: $P = \frac{(2.9CV^2)}{T}$ (Duty Cycle)
 (Output at Pin 10 and 11)

The circuit is designed so that most of the total power is consumed in the external components. In practice, the lower the values of frequency and voltage used, the closer the actual power dissipation will be to the calculated value.

Because the power dissipation does not depend on R , a design for minimum power dissipation would be a small value of C . The value of R would depend on the desired period (within the limitations discussed above).

7 - Timing-component limitations

The capacitor used in the circuit should be non-polarized and have low leakage (i.e. the parallel resistance of the capacitor should be an order of magnitude greater than the external resistor used). There is no upper or lower limit for either R or C value to maintain oscillation.

However, in consideration of accuracy, C must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account). R must be much larger than the COS/MOS "ON" resistance in series with it, which typically is hundreds of ohms. In addition, with very large values of R , some short-term instability with respect to time may be noted.

The recommended values for these components to maintain agreement with previously calculated formulas without trimming should be:

$C \geq 100 \text{ pF}$, up to any practical value, for astable modes;
 $C \geq 1000 \text{ pF}$, up to any practical value, for monostable modes.
 $10 \text{ K}\Omega \leq R \leq 1 \text{ M}\Omega$.