

This Specification contains a small amount of data which may not be legible. It has been acquired directly from the manufacturer or standards organization and Technical Indexes/IHS have not been able to obtain a better copy.

If the quality of this Specification is not fit for your intended purpose, please contact the relevant manufacturer or standards organization to clarify the details you require.

Specification available from:-

CONITATO ELETTROTECNICO ITALIANO - Viale Monza 259
20126 MILANO MI (Italy)

ISSUE 1 - 1987
July



Page 1 of 26 pages

ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH:

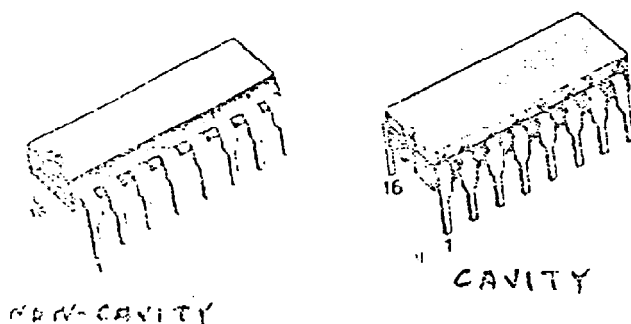
CECC 90 000 : 1985
CECC 90 100 : 1986

MANUFACTURERS TYPE NUMBER

4085B

Outline not to scale: Isometric projection
Marking information see page 9

SEE QPL CECC 00 200
For ordering information
see page 10



SILICON CMOS 4085 B WITH
BUFFERED OUTPUTS

DUAL 2-WIDE 2-INPUT
AND-OR INVERTER
GATE
CAVITY AND
NON-CAVITY PACKAGE

For detail dimensions see IEC 191-2 (A50C)

Assessment levels
R, S, T and V
and optional screening
categories A, B, C and D

CAUTION: THESE ARE STATIC SENSITIVE DEVICES - See clause 1.11

1. Limiting conditions of use (not for inspection purposes)

All voltages referenced to V_{SS}

- 1.1 Maximum supply voltage, positive
- 1.2 Maximum supply voltage, negative
- 1.3 Maximum positive input voltage
- 1.4 Maximum negative input voltage

V_{DD}	+18.0V
V_{DD}	-0.5V
V_I	V_{DD} +0.5V
V_I	-0.5V

1. Limiting conditions of use (contd)

1.5	Maximum power dissipation, per package per output	P_{D1} P_{D2}	200,0mW 50,0mW
1.6	Maximum continuous current into any input.	$ I_{I1} $	10,0mA
1.7	Maximum continuous current into any output.	$ I_{O1} $	10,0mA
1.8	Operating temperature range	T_{amb} Full Limited	 -55 to +125°C -40 to + 85°C
1.9	Storage temperature range	T_{stg}	-65 to +150°C
1.10	Transient energy rating		400V at 100pF through 1,5kΩ
1.11	<u>Recommended handling precautions</u>		
1.11.1	Store devices in either conductive foam or conductive rails, or connect all leads together using a similar electrical shorting method.		
1.11.2	Use grounded tip soldering irons.		
1.11.3	Ground all test equipment.		
1.11.4	Connect all unused device inputs to V_{DD} or V_{SS} .		
1.11.5	PC boards used to mount MOS devices should have all metal leads grounded during device mounting or flow soldering operations.		
1.11.6	Soldering equipment, solder pots or flow soldering equipment should be grounded whenever in contact with PC boards and/or MOS devices.		
1.11.7	Do not use ungrounded automatic insertion equipment or other handling equipment that precludes the use of suitable device lead grounding techniques during inspection or handling.		
1.11.8	When PC boards containing mounted MOS devices are removed from equipment for test, shipping or storage, 'Dummy connectors' should be used to electrically short all PC board terminals together.		
1.11.9	Switch off power supply before inserting or removing devices from circuits.		
1.11.10	Disconnect all low impedance equipment and input signals from the device before d.c. power supplies are switched off.		

2. Recommended conditions of use and associated characteristics (not for inspection purposes)

These apply over the operating temperature range unless otherwise stated. All voltages referenced to V_{SS} .

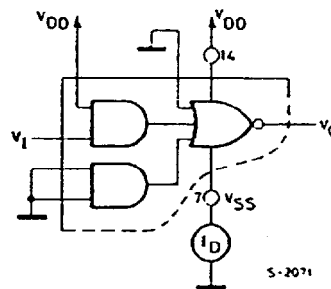
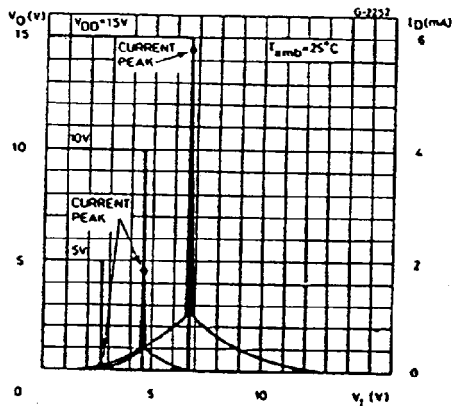
Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Quiescent device current	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range	Outputs open circuit	I_{DCA}	5,0	1,0	1,0	30,0	μA
		I_{DDA}	10,0	2,0	2,0	60,0	μA
		I_{DDA}	15,0	4,0	4,0	120,0	μA
Limited temperature range		I_{DDA}	5,0	4,0	4,0	30,0	μA
		I_{DDA}	10,0	8,0	8,0	60,0	μA
		I_{DDA}	15,0	16,0	16,0	120,0	μA
LOW level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OLA}	5,0	0,05	0,05	0,05	V
		V_{OLA}	10,0	0,05	0,05	0,05	V
		V_{OLA}	15,0	0,05	0,05	0,05	V
HIGH level output voltage at $ I_O < 1,0\mu A$	$V_{IL} = 0V$ $V_{IH} = V_{DD}$	V_{OHB}	5,0	4,95	4,95	4,95	V
		V_{OHB}	10,0	9,95	9,95	9,95	V
		V_{OHB}	15,0	14,95	14,95	14,95	V
LOW level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IL} = 1,5V$ $V_{IL} = 3,0V$ $V_{IL} = 4,0V$ —	V_{OLA}	5,0	0,5	0,5	0,5	V
		V_{OLA}	10,0	1,0	1,0	1,0	V
		V_{OLA}	15,0	1,5	1,5	1,5	V
HIGH level output voltage (for worst case combinations) at $ I_O < 1,0\mu A$	$V_{IH} = 3,5V$ $V_{IH} = 7,0V$ $V_{IH} = 11,0V$	V_{OHB}	5,0	4,5	4,5	4,5	V
		V_{OHB}	10,0	9,0	9,0	9,0	V
		V_{OHB}	15,0	13,5	13,5	13,5	V
Output LOW (sink) current							
Full temperature range	$V_O = 0,4V$ $V_O = 0,5V$ $V_O = 1,5V$	I_{OLB}	5,0	0,64	0,51	0,36	μA
		I_{OLB}	10,0	1,60	1,30	0,90	μA
		I_{OLB}	15,0	4,20	3,40	2,40	μA
Limited temperature range	$V_O = 0,4V$ $V_O = 0,5V$ $V_O = 1,5V$	I_{OLB}	5,0	0,52	0,44	0,36	μA
		I_{OLB}	10,0	1,30	1,10	0,90	μA
		I_{OLB}	15,0	3,60	3,00	2,40	μA

Characteristics	Conditions	Symbol	$V_{DD}(V)$	T_{amb} LOW	T_{amb} = 25°C	T_{amb} HIGH	Unit
Output HIGH (source) current							
Full temperature range	$V_O = 4,6V$	$-I_{OHB}$	5,0	0,64	0,51	0,36	mA
	$V_O = 9,5V$	$-I_{OHB}$	10,0	1,60	1,30	0,90	mA
	$V_O = 13,5V$	$-I_{OHB}$	15,0	4,20	3,40	2,40	mA
Limited temperature range	$V_O = 4,6V$	$-I_{OHB}$	5,0	0,52	0,44	0,36	mA
	$V_O = 9,5V$	$-I_{OHB}$	10,0	1,30	1,10	0,90	mA
	$V_O = 13,5V$	$-I_{OHB}$	15,0	3,60	3,00	2,40	mA
Input leakage current	$V_{IL} = 0V$ $V_{IH} = V_{DD}$						
Full temperature range		$ I_{IA} $	15,0	0,10	0,10	1,00	μA
Limited temperature range		$ I_{IA} $	15,0	0,30	0,30	1,00	μA
Input capacitance per unit load (Any input)	$V_I = 0V$ $f = 1MHz$	C_{IA}	-	-	7,5	-	pF
Noise margin at LOW level output (equal to the difference between V_{IL} and V_{OL} for worst case combinations)		V_{NLB}	5,0	1,0	1,0	1,0	V
		V_{NLB}	10,0	2,0	2,0	2,0	V
		V_{NLB}	15,0	2,5	2,5	2,5	V
Noise margin at HIGH level output (equal to the difference between V_{IH} and V_{OH} for worst case combinations)		V_{NHB}	5,0	1,0	1,0	1,0	V
		V_{NHB}	10,0	2,0	2,0	2,0	V
		V_{NHB}	15,0	2,5	2,5	2,5	V
Propagation and Transition Times	$C_L = 50pF$ (Test conditions as in Sub-group A5)						

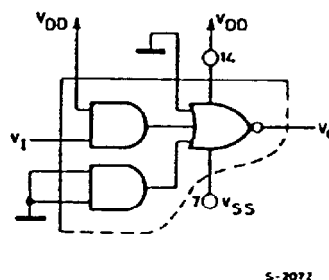
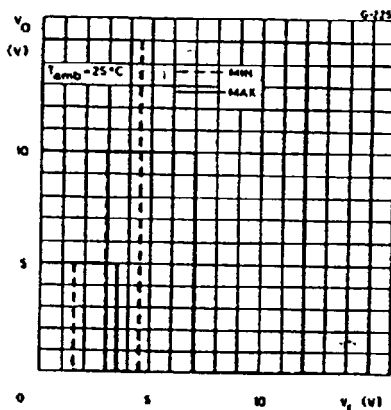
DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$, typical temperature coefficient for all V_{DD} values is $0.3\%/^{\circ}\text{C}$, all input rise and fall times = 20 ns)

Parameter	Test conditions	Values			Unit
		$V_{DD} \text{ (V)}$	Min.	Typ.	Max.
t_{PHL} Propagation delay time (Data)		5		225	450
		10		90	180
		15		65	130
t_{PLH} Propagation delay time (Data)		5		310	620
		10		125	250
		15		90	180
t_{PHL} Propagation delay time (Inhibit)		5		150	300
		10		60	120
		15		40	80
t_{PLH} Propagation delay time (Inhibit)		5		250	500
		10		100	200
		15		70	140
t_{TLH} , t_{THL} Transition time		5		100	200
		10		50	100
		15		40	80

Typical voltage and current transfer characteristics with test circuit

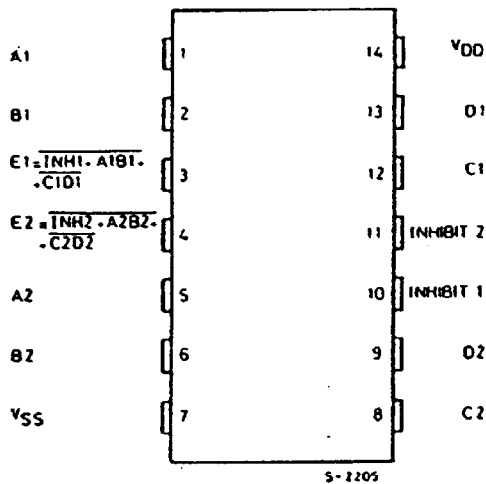


Minimum and maximum voltage transfer characteristics with test circuit

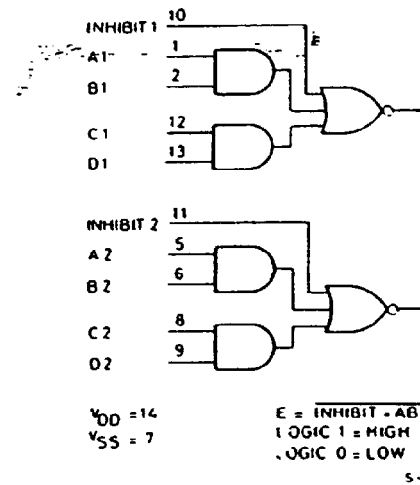


(5) The maximum usable resistance R_X is a function of the leakage of capacitance C_X , the leakage of the device, and the leakage due to board layout and surface resistance

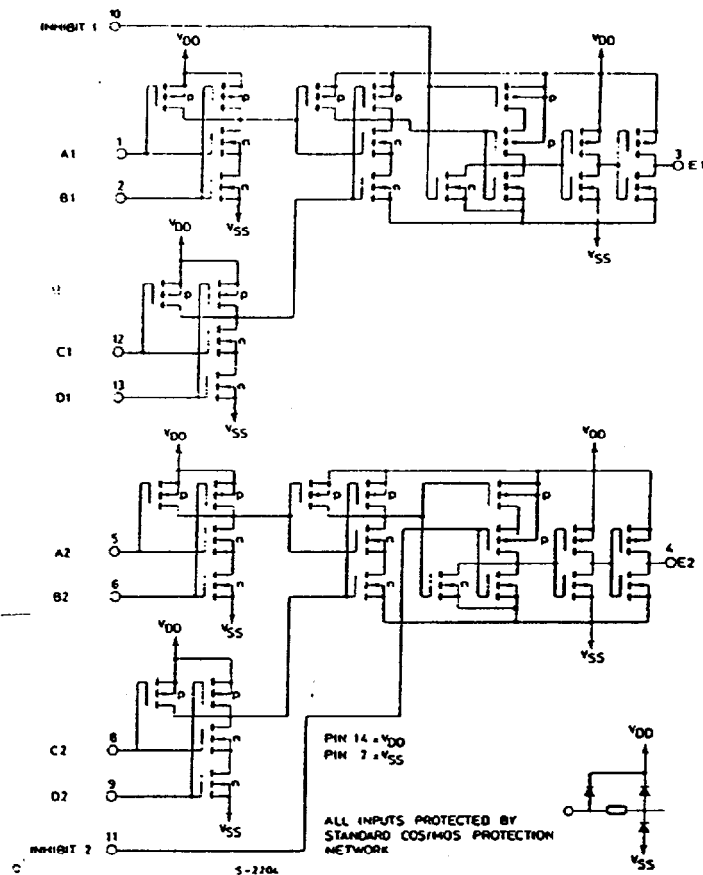
CONNECTION DIAGRAM



LOGIC DIAGRAM

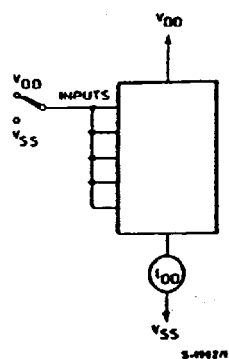


SCHEMATIC DIAGRAM

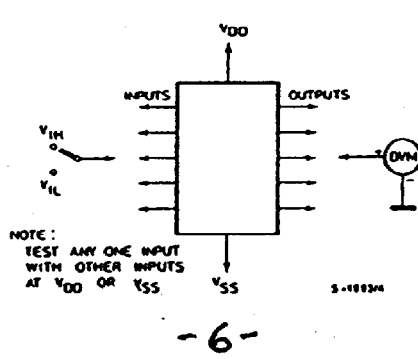


TEST CIRCUITS

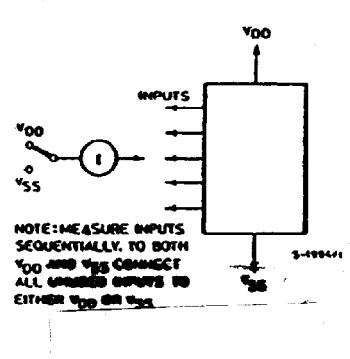
Quiescent device current



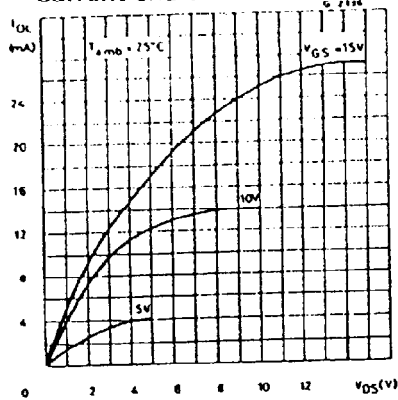
Input voltage



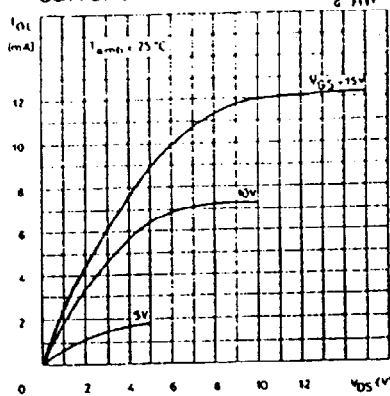
Input current



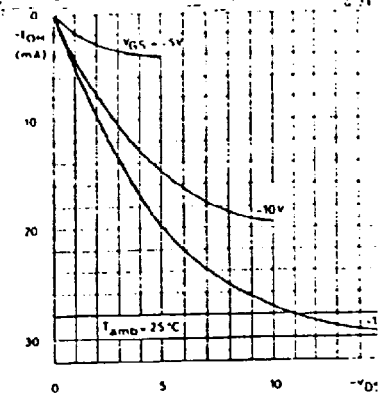
Typical output low (sink) current characteristics



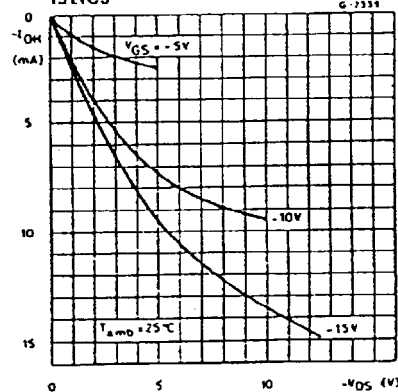
Minimum output low (sink) current characteristics



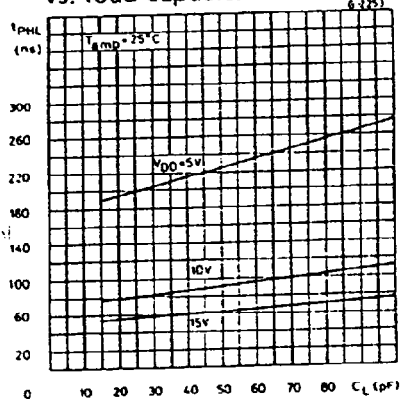
Typical output high (source) current characteristics



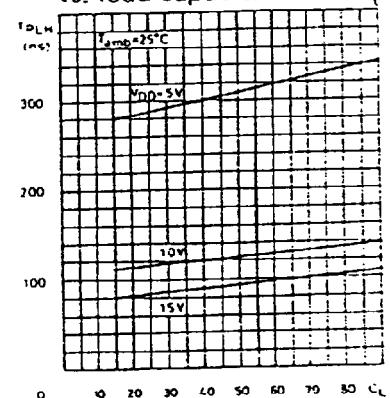
Minimum output high (source) current characteristics



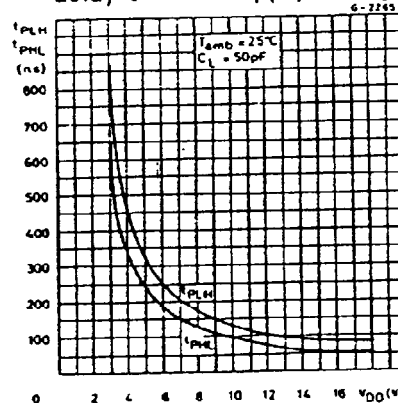
Typical data high-to-low level propagation delay time vs. load capacitance



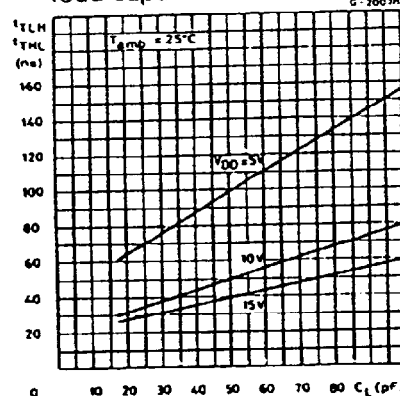
Typical data low-to-high level propagation delay time vs. load capacitance



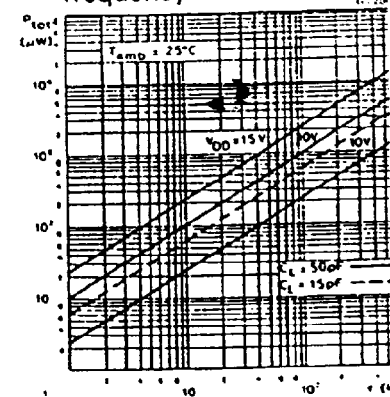
Typical data propagation delay time vs. supply voltage



Typical transition time vs. load capacitance



Typical power dissipation frequency



Marking

The following shall be marked on the device, in the following order of precedence, as space permits. All information, except the terminal marking shall appear on the primary package used as initial protection or wrapping for delivery:

- (1) Terminal identification
- (2) Type number
- (3) Operating temperature range (if not included in 2)
- (4) Quality assessment level applied
- (5) Screening class applied
- (6) Date-code (year-week defined by three or four figures)
- (7) Mark of conformity (CECC logo)
- (8) Manufacturers name or trade mark (may include factory code)
- (9) Factory identification code
- (10) Package materials
- (11) Caution label for devices susceptible to damage by electrostatic discharge
- (12) Optional tests