

NEDERLANDS ELEKTROTECHNISCH
COMITE
POSTBOX 5059
2600 GB DELFT

This specification is also available from
Nederlandse Philips Bedrijven B.V.

CECC 90 104-238



ISSUE 1

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Total number of pages: 14

ELECTRONIC COMPONENTS OF ASSESSED QUALITY IN ACCORDANCE WITH:

GS: CECC 90 000 Issue 4.
SS: CECC 90 100 Issue 3.
FS: CECC 90 104 Issue 2.

Detail Spec: NL-CECC 90 104-238
Issue: 1
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OUTLINE AND DIMENSIONS:

IEC 191-2 } 050 G011

TERMINAL CONNECTIONS:

See item 1.2 of this specification

DETAIL SPECIFICATION FOR
DIGITAL INTEGRATED CIRCUITS
IN ACCORDANCE WITH FS 90 104

HEC/HEF4753B

Universal timer module

TYPICAL CONSTRUCTION:

Silicon monolithic local oxidation
CMOS integrated circuit, cavity/non-
cavity packages.

CAUTION: STATIC SENSITIVE DEVICE

ASSESSMENT LEVELS: P, Y, L

REMARKS

Information about manufacturers who have components qualified to this detail specification is
available in the current CECC 00 200: Qualified Products List.

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1 TYPE DESCRIPTION

1.1 Function

The HEF4753B is a universal timer module for counting and dividing as well as for event-recognition and manipulation of input sequences.

The following functions are included: synchronization and edge-detection of the input signal, programmable counter, clock divider with different lengths, operating mode decoder, control logic and output multiplexer.

Depending on the operating mode and the application, the circuit works as a presettable 8-bit counter with transient-pulse suppression, pulse duration selector divider, counter, positive or negative edge delaying module or low-frequency control circuit.

All manipulation possibilities depend on a time scaling, which is adjustable by the 8-bit programmable counter and the system clock. The system clock can be divided internally by 1, 16, 256 or 4096 as input clock for the counter. In all cases the manipulated input sequence appears at the only output OUT.

1.1.1 Function tables

inputs			operating mode
LFC	Y	Z	
L	L	H	counter
L	H	L	divider
H	H	L	delayed LOW to HIGH edge
H	L	H	delayed HIGH to LOW edge
H	H	H	transient pulse suppression
L	H	H	frequency recognition
LFC	L	L	digital pulse duration selector

H = HIGH state (the more positive voltage).
L = LOW state (the less positive voltage).

Programmable 8-bit counter *

inputs active LOW	value
A	1
B	2
C	4
D	8
E	16
F	32
G	64
H	128

12-bit predivider

W	X	clock for programmable counter CP/X
L	L	X = 1
L	H	X = 16
H	L	X = 256
H	H	X = 4096

* All inputs A to H HIGH is not allowed.

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1.1.2 Functional diagram

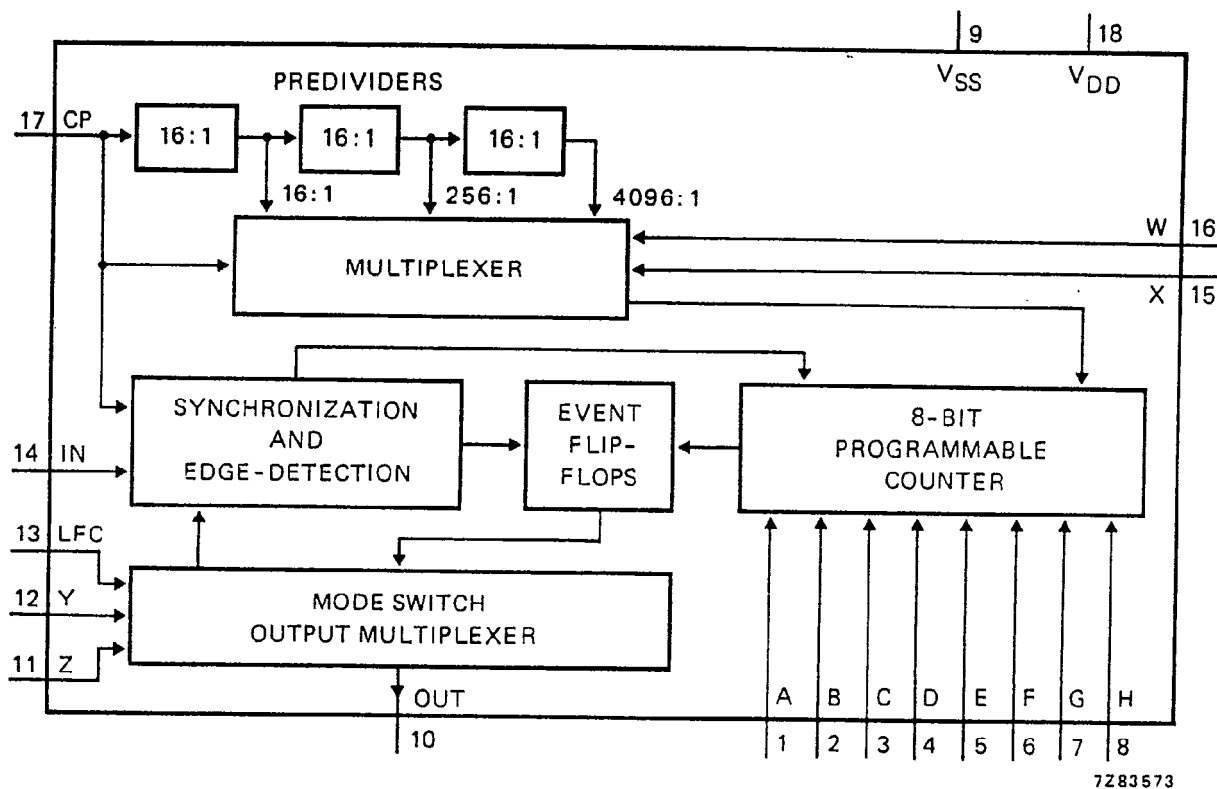


Fig.1 Functional diagram.

1.1.3 Pinning information

A to H	sets inputs for progr. 8-bit counter
VSS	ground
OUT	output
Z	operating mode inputs
Y	
LFC	
IN	input
W	frequency counter mode inputs
X	
CP	clock input
VDD	supply voltage

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1.1.4 Functional description

Clock divider and decoder

The clock signal at input CP is, at its original frequency, the system clock, but it also drives the programmable counter. The counter input frequency can be predivided by the factors 1/16, 1/256 and 1/4096, depending on the logic state of inputs W and X (according to the function tables above).

8-bit programmable counter

The 8 inputs A to H are the set inputs of the 8 counter flip-flops. The setting is triggered by an edge of the input signal (at input IN) depending on of the chosen mode.

Event flip-flops, synchronization and edge-detection

The event flip-flops are used to recognize the positive and/or negative edge of the input signal at IN. Parts of the flip-flops are used together with the programmable 8-bit counter as a retriggerable mono-flop, which defines the time scaling for event recognition. The input IN is synchronized by the clock signal CP.

Mode switch and output multiplexer

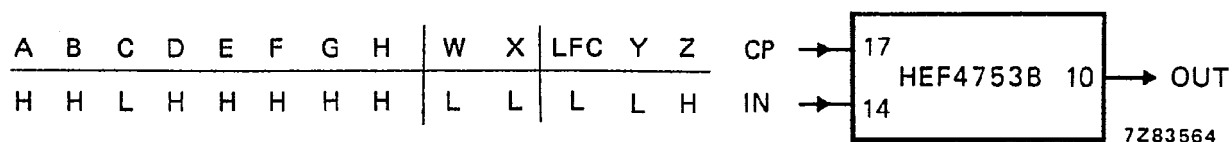
This function switches the chosen output to the output (OUT) and gives the mode of which the edge at input IN has to be detected. The inputs Z, Y and LFC give 7 modes +1, that means in mode 'Digital Filter' the input LFC can be HIGH or LOW.

OPERATING MODES

The circuit has 6 operating modes which are activated by the logic state of inputs LFC, Y and Z. An extra mode is possible by using two circuits which are connected such so they function as a digital band-filter.

1. Counter mode (LFC = LOW; Y = LOW; Z = HIGH)

In this mode the output OUT should be connected to input IN. If not, only one counter cycle starts after a transition at input IN (see Fig.2 and note 1).



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1.1.4 Functional description (continued)

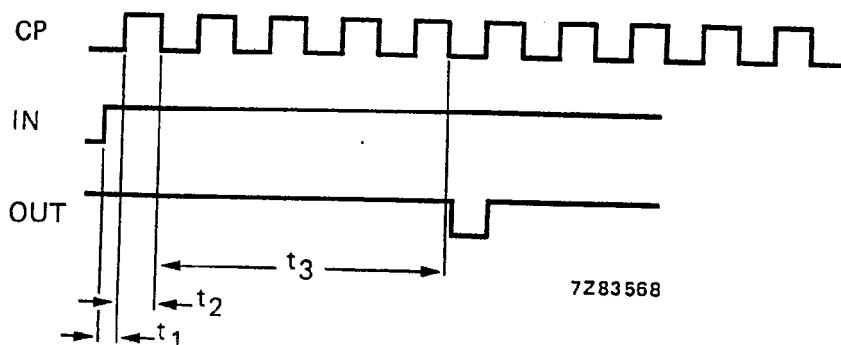


Fig.2 Timing diagram for counter mode; t_1 = delay until set of 8-bit counter; t_2 = delay to set 8-bit counter; t_3 = predefined delay by programming.

2. Divider mode (LFC = LOW; Y = HIGH; Z = LOW)

In this mode the output OUT should be connected to input IN. If not, only one counter cycle starts after a transition at input IN (see Fig.3 and note 1).

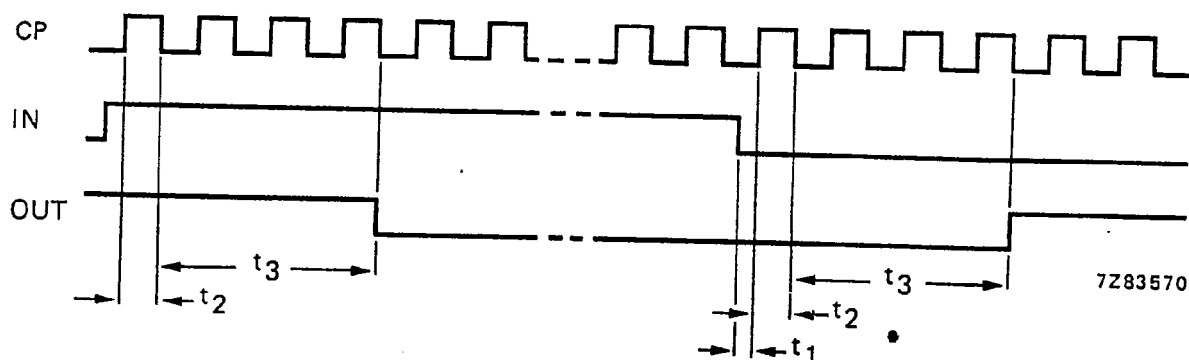
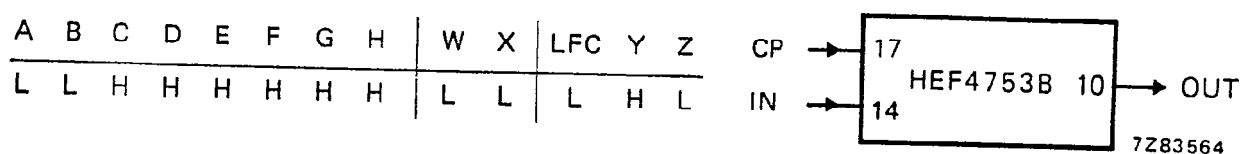


Fig.3 Timing diagram for divider mode; t_1 = delay until set of 8-bit counter; t_2 , t_3 see Fig.2.