

Förderverein für Elektrotechnische Normung (FEN) e. V.
Cenelec Electronic Components Committee

CECC

Système Harmonisé d'Assurance de la Qualité
des Composants Electroniques

SPECIFICATION DE FAMILLE:

**CIRCUITS INTEGRES
DIGITAUX C. MOS**

SERIES 4000 B ET 4000 UB

Harmonized System of Quality Assessment for
Electronic Components

FAMILY SPECIFICATION:

**C. MOS DIGITAL
INTEGRATED CIRCUITS**

SERIES 4000 B AND 4000 UB

Harmonisiertes Gütebestätigungssystem für
Bauelemente der Elektronik

FAMILIENSPEZIFIKATION:

**C. MOS DIGITALE
INTEGRIERTE SCHALTUNGEN**

SERIEN 4000 B UND 4000 UB



2 Edition
Issue
Ausgabe

CECC 90 104

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Information about the System may be obtained from:



FEN e.V. Secretariat
and
CECC General Secretariat
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or from the National Authorized Institutions
of the participating countries listed
who can supply copies of:

- 1 The Internal Regulations of the FEN e.V.
- 2 The Rules of Procedure of the System
- 3 CECC Specifications of the FEN and National Specifications for the System
- 4 CECC 00 200: Qualified Products List (QPL)
- 5 CECC 00 300: CECC Publications and their related national documents
- 6 Other CECC Publications and publicity documents

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FOREWORD

The CENELEC Electronic Components Committee (CECC) is composed of those member countries of the European Committee for Electrotechnical Standardization (CENELEC) who wish to take part in a harmonized System for electronic components of assessed quality.

The object of the System is to facilitate international trade by the harmonization of the specifications and quality assessment procedures for electronic components, and by the grant of an internationally recognized Mark, or Certificate, of Conformity. The components produced under the System are thereby acceptable in all member countries without further testing.

This specification has been formally approved by the CECC, and has been prepared for those countries taking part in the System who wish to issue national harmonized specifications for DIGITAL INTEGRATED CIRCUITS. It should be read in conjunction with the current regulations for the CECC System.

At the date of printing of this specification, the member countries of the CECC are Austria, Belgium, Denmark, Finland, France, Germany, Ireland, Italy, the Netherlands, Norway, Portugal, Spain, Sweden, Switzerland and the United Kingdom, and copies of it can be obtained from the addresses shown on the blue fly sheet.

PREFACE

This family specification was prepared by CECC WG 9: Integrated Circuits.

It contains the general information for the C.MOS series 4000 B and 4000 UB. Together with the device type detail specification, usually prepared nationally, it forms the complete detail specification for the devices belonging to series 4000 B and 4000 UB.

It is based, wherever possible, on the Publications of the International Electrotechnical Commission.

The text of this specification was circulated to the CECC for voting in the document indicated below and was ratified by the President of the CECC for printing as a CECC Specification.

<u>Document</u>	<u>Date of Voting</u>	<u>Report on the Voting</u>
CECC(Secretariat)2373	March 1989	CECC(Secretariat)2447

In accordance with the decision of the CECC Management Committee this specification is published initially in English and French. The German text will follow as soon as it has been prepared.

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ELECTRONIC COMPONENTS OF ASSESSED QUALITY IN ACCORDANCE WITH :

GS : CECC 90 000 : Generic Specification for Monolithic Integrated
Circuits

SS : CECC 90 100 : Sectional Specification for Digital Monolithic
Integrated Circuits

OUTLINE AND DIMENSIONS

In accordance with IEC 191-2

See detail specification of the
specific type

Terminal connections, lead plating
and material :

see detail specification of the
specific type

FAMILY SPECIFICATION

For C.MOS 4000 B and 4000 UB Series,
digital integrated circuits

TYPICAL CONSTRUCTION :

Silicon complementary MOS,
buffered (B) and unbuffered (UB)
outputs, cavity and non cavity
packages

NOTATION : THESE STATIC
SENSITIVE DEVICES

ASSESSMENT LEVELS :

P, Y, L

LIMITING CONDITIONS OF USE FOR THE FAMILY (not for the selection purposes)

Maximum supply voltage, positive	$V_{DD} = + 18 \text{ V}$	
Maximum supply voltage, negative	$V_{DD} = - 0,5 \text{ V}$	
Maximum positive input voltage	$V_I = V_{DD} + 0,5 \text{ V}$	} See Note 1
Maximum negative input voltage	$V_I = - 0,5 \text{ V}$	

Information about manufacturers who have components qualified to a detail
specification written in accordance with this family specification is
given in the current CECC 00 200 : Qualified Products List.

- 1.5 Maximum power dissipation per output and per package See detail specification
- 1.6 Maximum continuous current (any input) $|I| = 10 \text{ mA}$
- 1.7 Maximum continuous current into any output See detail specification
- 1.8 Operating temperature range T_{amb} Full = - 55 to + 125 °C
Limited = - 40 to + 85 °C
- 1.9 Storage temperature range T_{stg} - 65 to + 150 °C
- 1.10 Transient energy rating See detail specification

Note 1 : Except for transient (see 1.10 and 2.14.2)

2 RECOMMENDED OPERATING CONDITIONS AND ASSOCIATED CHARACTERISTICS FOR THE FAMILY (not for inspection purposes)

These apply over the operating temperature range, unless otherwise stated.
All voltages are referenced to V_{SS}

Symbol	$V_{\text{DD}}(\text{V})$	$T_{\text{amb}} = T_{\text{amb min.}}$	$T_{\text{amb}} = +25 \text{ °C}$	$T_{\text{amb}} = T_{\text{amb max.}}$	Unit
2.1 Quiescent device current $V_{\text{IL}} = 0 \text{ V}$ $V_{\text{IH}} = V_{\text{DD}}$ All valid input combinations					
2.1.1 For full operating temperature range *)					
- Gates	5 10 15	0,25 0,5 1	0,25 0,5 1	7,5 15 30	
- Buffers, flip-flops	5 10 15	1 2 4	1 2 4	30 60 120	
- MSI	5 10 15	5 10 20	5 10 20	150 300 600	

*) The detail specification shall specify the applicable group

2.1.2 For limited
operating
temperature
range *)

- LSI

- Gates

- Buffers,
flip-flops

- MSI

- LSI

2.2 Low level
output
voltage
 $V_{IL} = 0 \text{ V}$,
 $V_{IH} = V_{DD}$
 $|I_O| < 1 \mu\text{A}$

2.3 High level
output voltage
 $V_{IL} = 0 \text{ V}$,
 $V_{IH} = V_{DD}$
 $|I_O| < 1 \mu\text{A}$

2.4 Low or high
level output
voltage
applies for
worst case
input
conditions

Symbol	$V_{DD}(\text{V})$	$T_{\text{amb}} =$ $T_{\text{amb min.}}$	$T_{\text{amb}} =$ $+25 \text{ }^\circ\text{C}$	$T_{\text{amb}} =$ $T_{\text{amb max.}}$	Unit
I_{DDA}	5	15	15	375	μA
	10	25	25	750	
	15	50	50	1500	
	5	1	1	7,5	
	10	2	2	15	
	15	4	4	30	
	5	4	4	30	
	10	8	8	60	
	15	16	16	120	
	5	20	20	150	
	10	40	40	300	
	15	80	80	600	
	5	50	50	375	
	10	100	100	750	
	15	200	200	1500	
V_{OLA}	5	0,05	0,05	0,05	V
	10	0,05	0,05	0,05	
	15	0,05	0,05	0,05	
V_{OHB}	5	4,95	4,95	4,95	V
	10	9,95	9,95	9,95	
	15	14,95	14,95	14,95	

*) The detail specification shall specify the applicable group

2.4.1 B series

Low or high
level output
voltage at
 $|I_O| < 1 \mu A$

$V_{IL} = 1,5 \text{ V}$

for

$V_{DD} = 5 \text{ V}$

$V_{IL} = 3,0 \text{ V}$

for

$V_{DD} = 10 \text{ V}$

$V_{IL} = 4,0 \text{ V}$

for

$V_{DD} = 15 \text{ V}$

$V_{IH} = 3,5 \text{ V}$

for

$V_{DD} = 5 \text{ V}$

$V_{IH} = 7,0 \text{ V}$

for

$V_{DD} = 10 \text{ V}$

$V_{IH} = 11,0 \text{ V}$

for

$V_{DD} = 15 \text{ V}$

2.4.2 UB series

Low or high
level output
voltage at
 $|I_O| < 1 \mu A$

$V_{IL} = 1,0 \text{ V}$

for

$V_{DD} = 5 \text{ V}$

$V_{IL} = 2,0 \text{ V}$

for

$V_{DD} = 10 \text{ V}$

$V_{IL} = 2,5 \text{ V}$

for

$V_{DD} = 15 \text{ V}$

Symbol	$V_{DD}(\text{V})$	$T_{\text{amb}} =$ $T_{\text{amb min.}}$	$T_{\text{amb}} =$ $+25^\circ \text{C}$	$T_{\text{amb}} =$ $T_{\text{amb max.}}$	Unit
V_{OLA}	5	0,5	0,5	0,5	V
	10	1,0	1,0	1,0	
	15	1,5	1,5	1,5	
V_{OHB}	5	4,5	4,5	4,5	V
	10	9,0	9,0	9,0	
	15	13,5	13,5	13,5	
V_{OLA}	5	0,5	0,5	0,5	V
	10	1,0	1,0	1,0	
	15	1,5	1,5	1,5	

$V_{IH} = 4,0 \text{ V}$
 for
 $V_{DD} = 5 \text{ V}$
 $V_{IH} = 8,0 \text{ V}$
 for
 $V_{DD} = 10 \text{ V}$
 $V_{IH} = 12,5 \text{ V}$
 for
 $V_{DD} = 15 \text{ V}$

2.5 Output low
 (sink)
 current
 (see note 2)
 $V_{IL} = 0 \text{ V}$,
 $V_{IH} = V_{DD}$

2.5.1 For full
 temperature
 range
 $V_O = 0,4 \text{ V}$
 $V_O = 0,5 \text{ V}$
 $V_O = 1,5 \text{ V}$

2.5.2 For limited
 temperature
 range
 $V_O = 0,4 \text{ V}$
 $V_O = 0,5 \text{ V}$
 $V_O = 1,5 \text{ V}$

2.6 Output high
 (source)
 current (see
 note 2 and
 note 3)
 $V_{IL} = 0 \text{ V}$,
 $V_{IH} = V_{DD}$

Symbol	$V_{DD}(\text{V})$	$T_{amb} =$ $T_{amb \text{ min.}}$	$T_{amb} =$ $+25 \text{ } ^\circ\text{C}$	$T_{amb} =$ $T_{amb \text{ max.}}$	Unit
V_{OHB}	5	4,5	4,5	4,5	V
	10	9,0	9,0	9,0	
	15	13,5	13,5	13,5	
I_{OLB}	5	0,64	0,51	0,36	mA
	10	1,6	1,3	0,9	
	15	4,2	3,4	2,4	
	5	0,52	0,44	0,36	
	10	1,3	1,1	0,9	
	15	3,6	3,0	2,4	

Note 2 : Unless otherwise specified in the detail specification

Note 3 : For devices with symmetrical outputs the values for I_{OHA} are equal to the negative values for I_{OLB}

2.6.1 For full temperature range

$V_O = 4,6 \text{ V}$

$V_O = 9,5 \text{ V}$

$V_O = 13,5 \text{ V}$

2.6.2 For limited temperature range

$V_O = 4,6 \text{ V}$

$V_O = 9,5 \text{ V}$

$V_O = 13,5 \text{ V}$

2.7 Input leakage current

$V_{IL} = 0 \text{ V},$

$V_{IH} = V_{DD}$

2.7.1 For full temperature range

2.7.2 For limited temperature range

2.8 Three -state output leakage current

$V_{IL} = 0 \text{ V},$

$V_{IH} = V_{DD}$

combined to obtain a high impedance output state

2.8.1 For full temperature range

2.8.2 For limited temperature range

2.9 Input capacitance per unit load (any input)

Symbol	$V_{DD}(\text{V})$	$T_{\text{amb}} = T_{\text{amb min.}}$	$T_{\text{amb}} = +25 \text{ }^{\circ}\text{C}$	$T_{\text{amb}} = T_{\text{amb max.}}$	Unit
I_{OHA}	5	- 0,25	- 0,2	- 0,14	mA
	10	- 0,62	- 0,5	- 0,35	
	15	- 1,8	- 1,5	- 1,1	
I_{OHA}	5	- 0,2	- 0,16	- 0,12	mA
	10	- 0,5	- 0,4	- 0,3	
	15	- 1,4	- 1,2	- 1,0	
$ I_I _A$	15	0,1	0,1	1,0	μA
	15	0,3	0,3	1,0	
$ I_{\text{oz}} _A$	15	0,4	0,4	12	μA
	15	1,6	1,6	12	
	15	1,6	1,6	12	
C_{IA}			7,5		pF

2.10 Noise margin
at low level
output (equal
to difference
between V_{IL}
and V_{OL}
values as
given in 2.4)

2.10.1 B series

2.10.2 UB series

2.11 Noise margin
at high level
output (equal
to difference
between V_{IH}
and V_{OH}
values as
given in 2.4)

2.11.1 B series

2.11.2 UB series

2.12 Supply
voltage
range
(verification
of the
function at:
 $V_{DD} = 5; 10$
and 15 V)

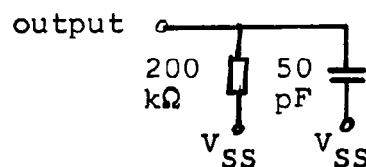
Symbol	$V_{DD}(V)$	$T_{amb} =$ $T_{amb \text{ min.}}$	$T_{amb} =$ $+25^{\circ}C$	$T_{amb} =$ $T_{amb \text{ max.}}$	Unit
V_{NLB}					V
	5	1	1	1	
	10	2	2	2	
	15	2,5	2,5	2,5	
	5	0,5	0,5	0,5	
	10	1	1	1	
V_{NHB}	15	1	1	1	V
	5	1	1	1	
	10	2	2	2	
	15	2,5	2,5	2,5	
	5	0,5	0,5	0,5	
	10	1	1	1	
V_{DDB}		+3	+3	+3	V
		+15	+15	+15	

2.13 Propagation and transition times

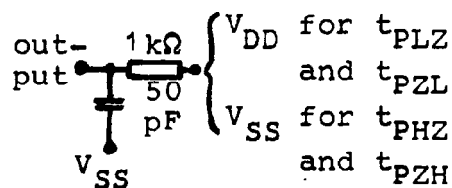
Symbol	$V_{DD}(V)$	$T_{amb} = T_{amb \text{ min.}}$	$T_{amb} = +25^{\circ}C$	$T_{amb} = T_{amb \text{ max.}}$	Unit
t_{PLHA} t_{PHLA} t_{TLHA} t_{THLA} t_{PHZA} t_{PZHA} t_{TLZA} t_{TZLA} t_{PLZA} t_{PZLA} t_{THZA} t_{TZHA}	5, 10 and 15	see relevant detail specification			ns

Load networks:

For normal outputs:



For three state outputs:



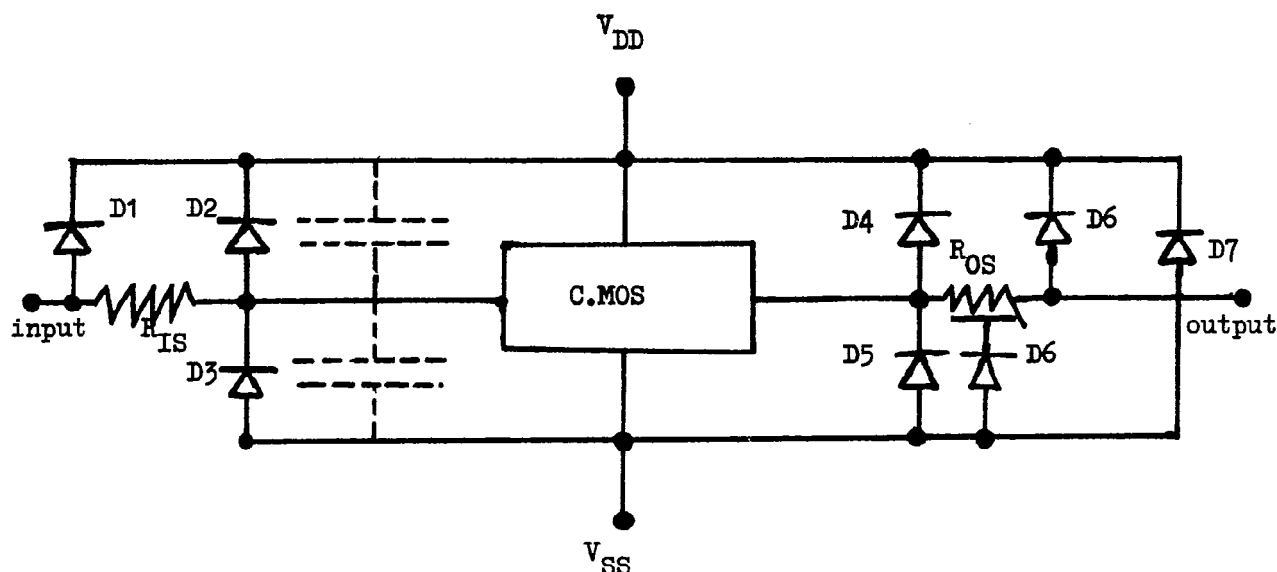
2.14 Supplementary information

2.14.1 Unused inputs:

Unused inputs shall be connected to the appropriate logic voltage (e.g. either V_{SS} or V_{DD} or associated input).

2.14.2 Transient energy protection

C.MOS circuits have built-in protection circuits on all inputs to reduce the possibility of damage to the input gate oxide of the device by the transfer of electrostatic charge. Output gates may be similarly protected. A schematic may be given, for example:



Generally used values: (see also relevant detail specification)

$$R_{IS} = 200 \text{ to } 2000 \, \Omega \text{ nom}$$

$$R_{OS} = 10 \text{ to } 1000 \, \Omega \text{ nom}$$

$$BV_{D1} = 50 \text{ to } (80) \text{ to } 120 \text{ V}$$

$$BV_{D2} = 20 \text{ to } 50 \text{ V}$$

$$BV_{D3} = 20 \text{ to } 50 \text{ V}$$

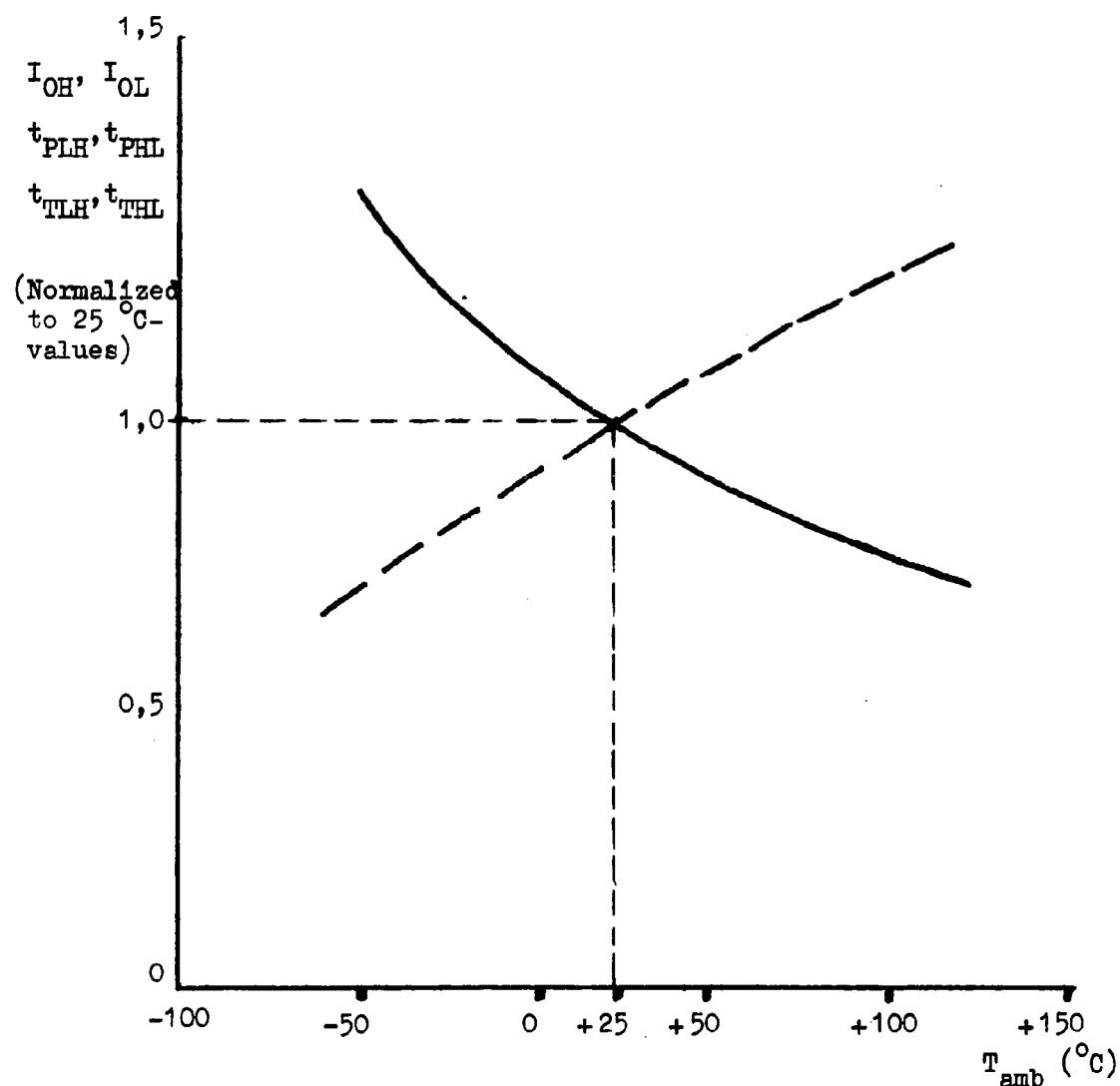
$$BV_{D4} = 20 \text{ to } 50 \text{ V}$$

$$BV_{D5} = 20 \text{ to } 50 \text{ V}$$

$$BV_{D6} = 50 \text{ to } (80) \text{ to } 120 \text{ V}$$

$$BV_{D7} = 20 \text{ to } 50 \text{ V}$$

2.14.3 Variation of parameters with temperature should be given in the format shown below; the curves given here show the general trend.



I_{OH}, I_{OL} _____

t_{PHL}, t_{PLH} } _____
 t_{THL}, t_{TLH} }

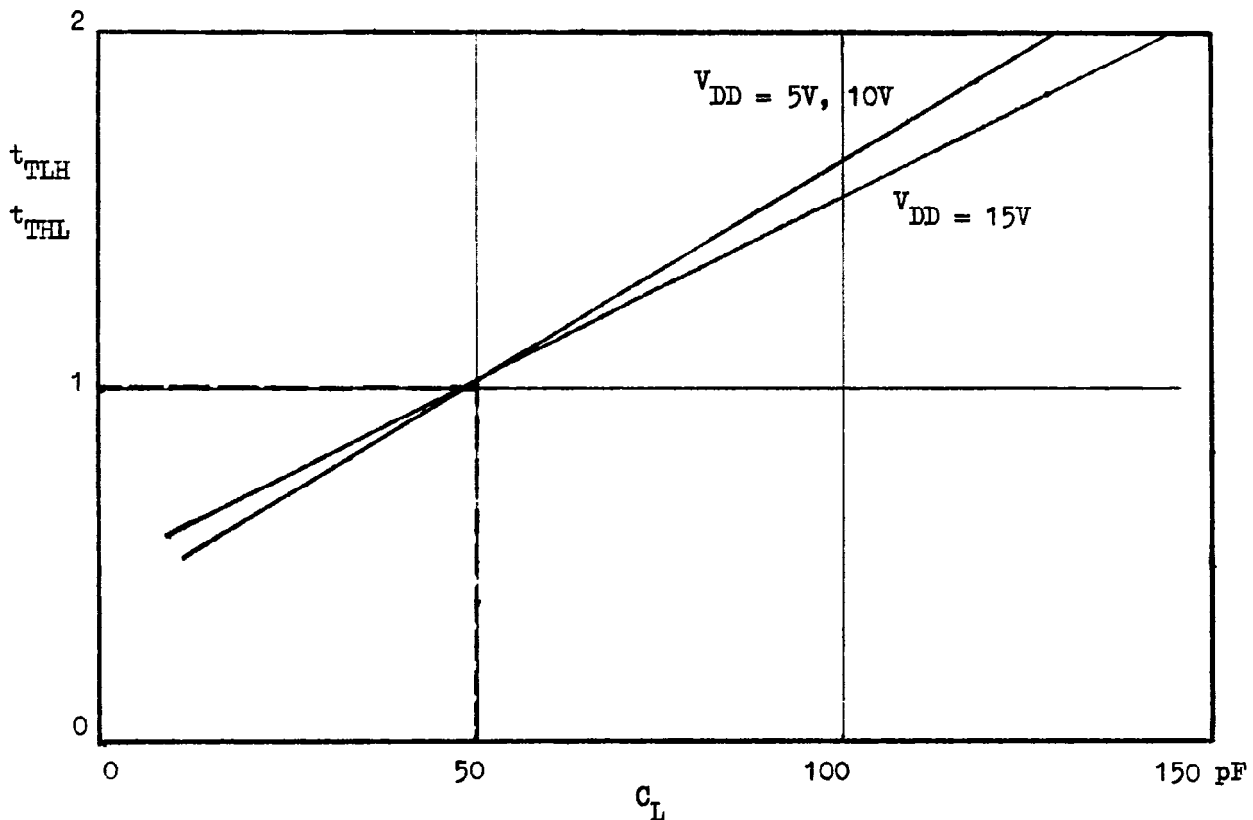
2.14.4 Variation of switching times with load capacitance shall be given in the detail specification.

Due to the very low input current requirements for C.MOS, there is practically no DC output loading capability limitation when driving other C.MOS inputs.

The actual fan-out of the C.MOS device is limited by a capacitance load consideration based on the desired system operating frequency.

The effects of capacitive load on the dynamic characteristics shall be given.

The curves shown below give the general trend of transition times versus load capacitance, which implies the general trend of propagation times versus load capacitance.



Normalized to $C_L = 50$ pF value

3 INSPECTION REQUIREMENTS

These requirements are given in the following tables and in the relevant DS.

NOTES :1 - All tests are performed at $T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise prescribed.

2 - In the tables the clause numbers refer to the generic, to the sectional or to this family specification with the following code :

GS : generic specification (CECC 90 000)

SS : sectional specification (CECC 90 100)

FS : family specification (CECC 90 104)

Example : GS/4.2.2 = 4.2.2 of CECC 90 000.

3 - The following abbreviations are used :

D : destructive test

ND : non-destructive test

IL : inspection level

AQL : acceptable quality level

n : sample size

c : acceptance criterion

na : not applicable