

BRITISH STANDARDS INSTITUTION
2, Park Street, London W1A 2BS

Specification available from :- As Shown in PD9002,
and CECC 00 200 and

NATIONAL SEMICONDUCTOR (UK) Ltd.

Larkfield Industrial Estate,

Greenock, Scotland

BS CECC 90105 - 007

Issue 1

September 1985



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ELECTRONIC COMPONENTS OF ASSESSED QUALITY
DETAIL SPECIFICATION IN ACCORDANCE WITH

GS: BS CECC 90000 Issue 2

SS: BS CECC 90100 Issue 2

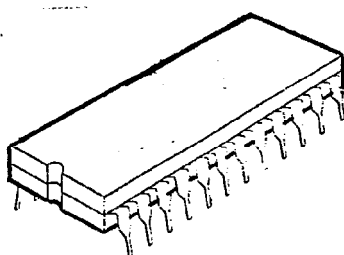
MANUFACTURER'S
TYPE NUMBER

DM54S474J

DM54S474BJ

Outline NOT TO SCALE Isometric projection
For dimensions see IEC 191-2 (A50G)

For Ordering Information
see clause 5



J Package

512 X 8 BIT SCHOTTKY TTL
PROGRAMMABLE READ-ONLY
MEMORY WITH TRI-STATE
OUTPUTS

TYPICAL CONSTRUCTION:
MONOLITHIC INTEGRATED
CIRCUIT, DUAL-IN-LINE
HERMETICALLY SEALED
ENCAPSULATION

ASSESSMENT LEVEL:

R

Terminal connections: See figure 1

For Marking Information See clause 1.3.3

1. Functional Description

The DM54S474 is a 4096 bit programmable read-only memory (PROM) organised as 512, 8 bit words. It features SCHOTTKY clamping for high speed, advanced titanium-tungsten (Ti-W) fuse links, low current PNP inputs to reduce loading, and Three-state outputs. The DM54S474 is TTL compatible.

The address inputs are decoded on-chip. Four memory enable inputs are provided to control the output states. When $\overline{E1}$ and $\overline{E2}$ are low and $E3$ and $E4$ are high, the output presents the contents of the selected word. If $\overline{E1}$ or $\overline{E2}$ are high, or $E3$ or $E4$ are low, it causes all 8 outputs to go to the high impedance state.

In the unprogrammed condition a logic LOW level will be produced at the output.

Refer to Qualified Product List PD 9002 and CECC 00200 for details of manufacturers approved to this specification.



Documents

Document Sharing Hub

1.2.3 Block Diagram

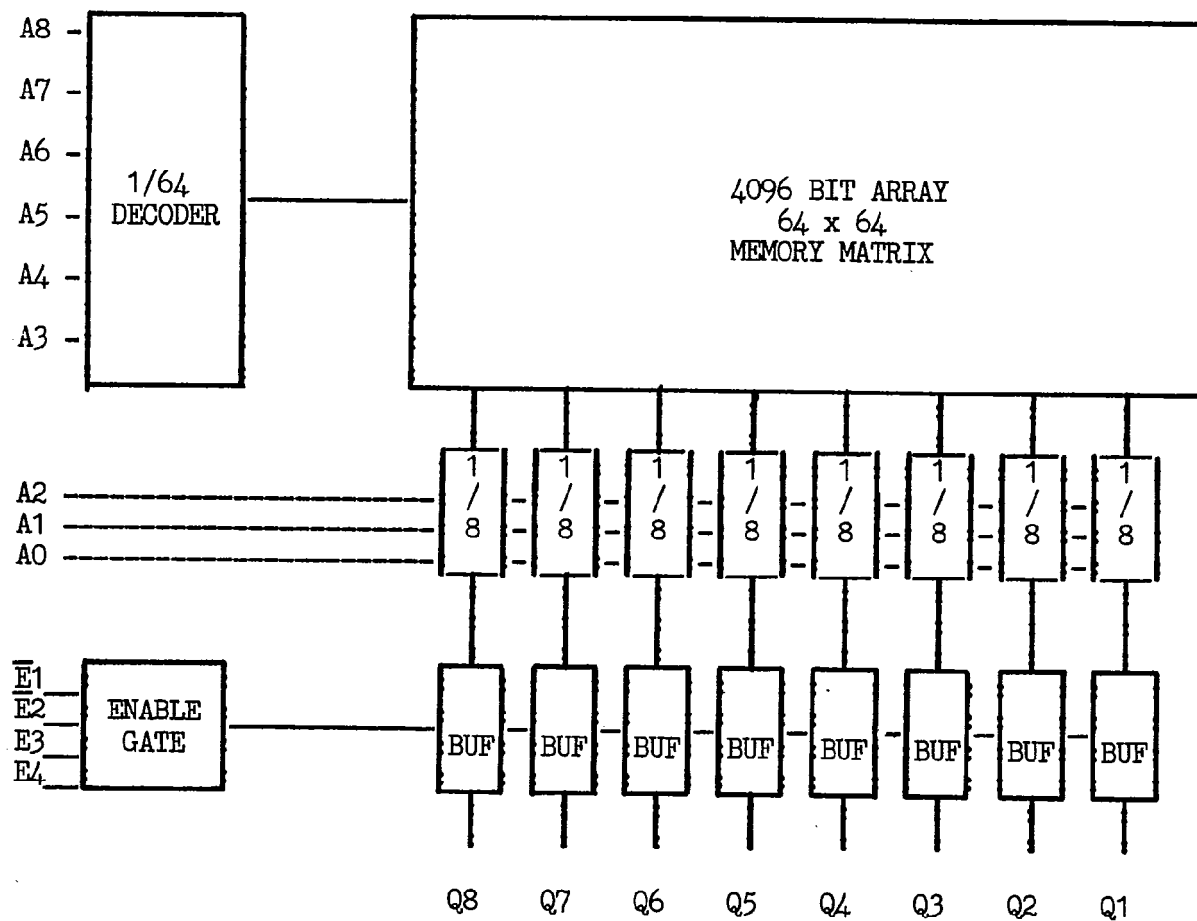
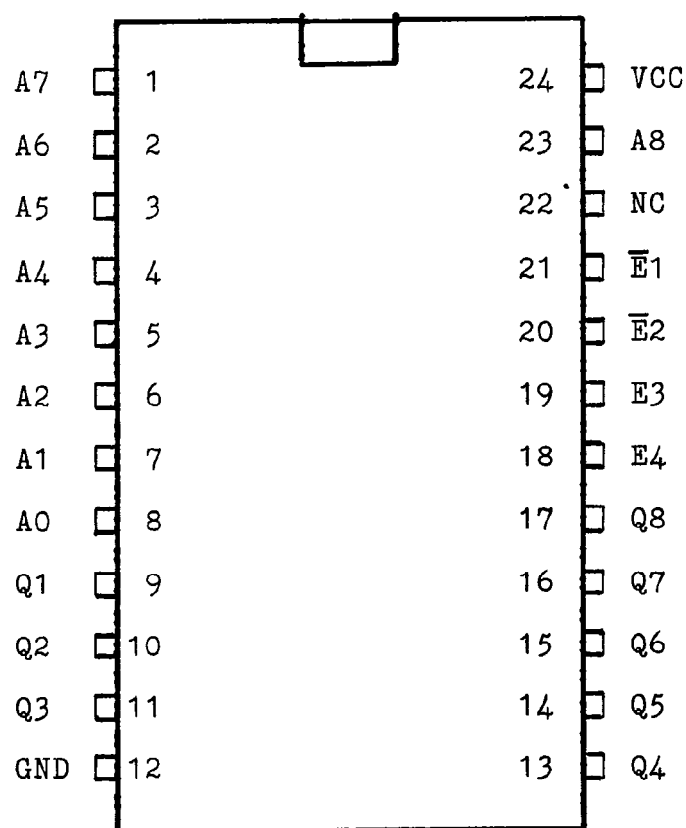


FIG. 2

1.3 Terminal Identification, Type Designation and Marking.

1.3.1 Terminal Identification (top view) and pin definitions.



Pin	Name	Function
A0 to A8		Address Inputs
Q1 to Q8		Data Outputs
E1, E2, E3, E4		Enable Inputs

FIG. 3

1.3.2 Type Designation

DM54S474J

4K bit (512 X 8) Schottky TTL Fusible Link PROM with three-state outputs.

DM54S474BJ

As above with speed selection (see 3.3.2)

1.3.3 Marking

Each Integrated Circuit shall bear the following marking:

- a. Terminal Identification
- b. Type Number
- c. Factory Identification Code
- d. Date Code
- e. Screening Class
- f. Assessment Level

1.4 Ordering Information

1. Manufacturer's Part Number
2. Required Quality Assessment Level
3. Relevant Screening Class (see addendum 1 to BS CECC 90000)
4. Relevant DS Number, Issue and Date.

2. LIMITING CONDITIONS OF USE (not for inspection purposes)

2.1 READ MODE

CHARACTERISTIC	:	SYMBOL	:	MIN	:	MAX	:	UNIT
Supply Voltage	:	V_{CC}	:	-0.5	:	+7.0	:	V
Input Voltage	:	V_I	:	-1.2	:	+5.5	:	V
Output Voltage appl.	:	V_O	:	-0.5	:	+5.5	:	V
Max. Power Dissipation	:	P_{tot}	:		:	1.0	:	W
Operating Temperature	:	T_{amb}	:	-55.0	:	+125.0	:	°C
Storage Temperature	:	T_{stg}	:	-65.0	:	+150.0	:	°C

2.2 PROGRAMMING MODE

CHARACTERISTIC	:	SYMBOL	:	MIN	:	MAX	:	UNIT
Supply Voltage	:	V_{CCP}	:	10.0	:	11.0	:	V
Input Voltage (Address and Enable Inputs)	:	V_I	:	0.0	:	+5.5	:	V
Output Voltage appl.	:	V_O	:	10.0	:	11.0	:	V
Max. Power Dissipation	:	P_{tot}	:		:	1.0	:	W
Operating Temperature	:	T_{amb}	:	+15.0	:	+30.0	:	°C

3. RECOMMENDED OPERATING CONDITIONS, PROGRAMMING CHARACTERISTICS AND ASSOCIATED CHARACTERISTICS. (not for inspection purposes)

3.1 Recommended Operating Conditions

The following conditions and characteristics apply over the operating temperature range and supply voltage range specified.

For programming conditions see clause 3.2. For read conditions see clause 3.3.

3.2 Programming Mode.

3.2.1 Programming Conditions and Characteristics.

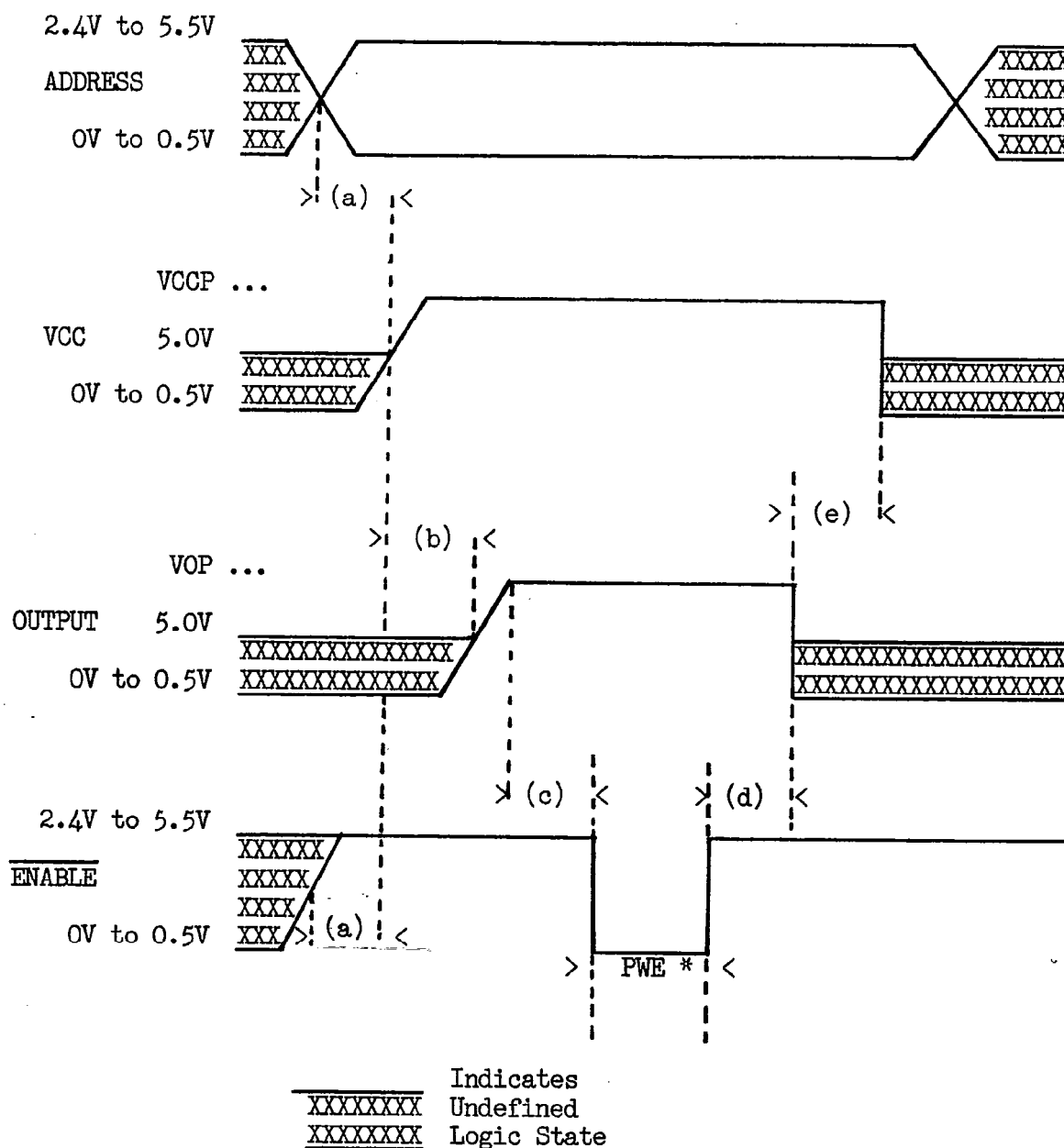
CHARACTERISTIC	CONDITIONS	SYMBOL	MIN	MAX	UNIT
Operating Temperature		T_{amb}	15.0	30.0	$^{\circ}C$
Power Supply Voltage to Program		V_{CCP}	10.0	11.0	V
Low Power Supply Voltage to Verify		V_{CCVL}	3.8	4.2	V
High Power Supply Voltage to Verify		V_{CCVH}	5.8	6.2	V
Programming Supply Current	$V_{CCP} = 11.0V$	I_{CCP}		750	mA
Input High Voltage		V_{IH}	2.4	5.5	V
Input Low Voltage		V_{IL}		0.8	V
Forced Output Voltage		V_{OPF}	10.0	11.0	V
Programming Output Current	$V_O = 11V$	I_{OPF}		20.0	mA
CE Input High Voltage		V_{IHCE}	2.4	5.5	V
CE Input Low Voltage		V_{ILCE}	0.0	0.8	V
Applied Output Voltage or Supply Voltage Slew Rate		t_{sr}	1.0	10.0	V/us
CE Programming Pulse Width (enabled)		PWE	9.0	11.0	us

3.2.1. cont.

CHARACTERISTIC	CONDITIONS	SYMBOL	MIN	MAX	UNIT
Pulse Sequence Delay		t_d	33.0		us
Duty Cycle for V_{cc} at V_{ccp}	M_{DC}			25.0	%
Max. fusing attempts per link to achieve the min. yield		F_L		10	
Minimum Programming Yield		P_Y	90		%
Set-Up time of Address		t_{sadd}	100		ns
Set-Up time of Program V_{cc}		$t_{sV_{ccp}}$	5 *		us
Set-Up time of Output voltage		$t_{sV_{op}}$	100		ns
Hold-time of Output voltage		$t_{hV_{op}}$	100		ns
Hold time of Program V_{cc}		$t_{hV_{ccp}}$	100		ns
Total Programming time for each location: (Excluding Verify time)			65		us

* May be >0 if V_{ccp} rises at the same rate or faster than V_{op}

3.2.2 Programming Waveforms



* PWE is repeated for 5 additional pulses after verification of V_{OH} indicates a bit has been programmed.

- (a) t_{sadd} Set-up time of address before program V_{CC} set.
- (b) t_{sVccp} Set-up time of program V_{CC} before output program voltage set.
- (c) t_{sVop} Set-up time of output voltage before program pulse.
- (d) t_{hVop} Hold time of output after program pulse.
- (e) t_{hVccp} Hold time of program V_{CC} after output program voltage removed.

FIG. 4